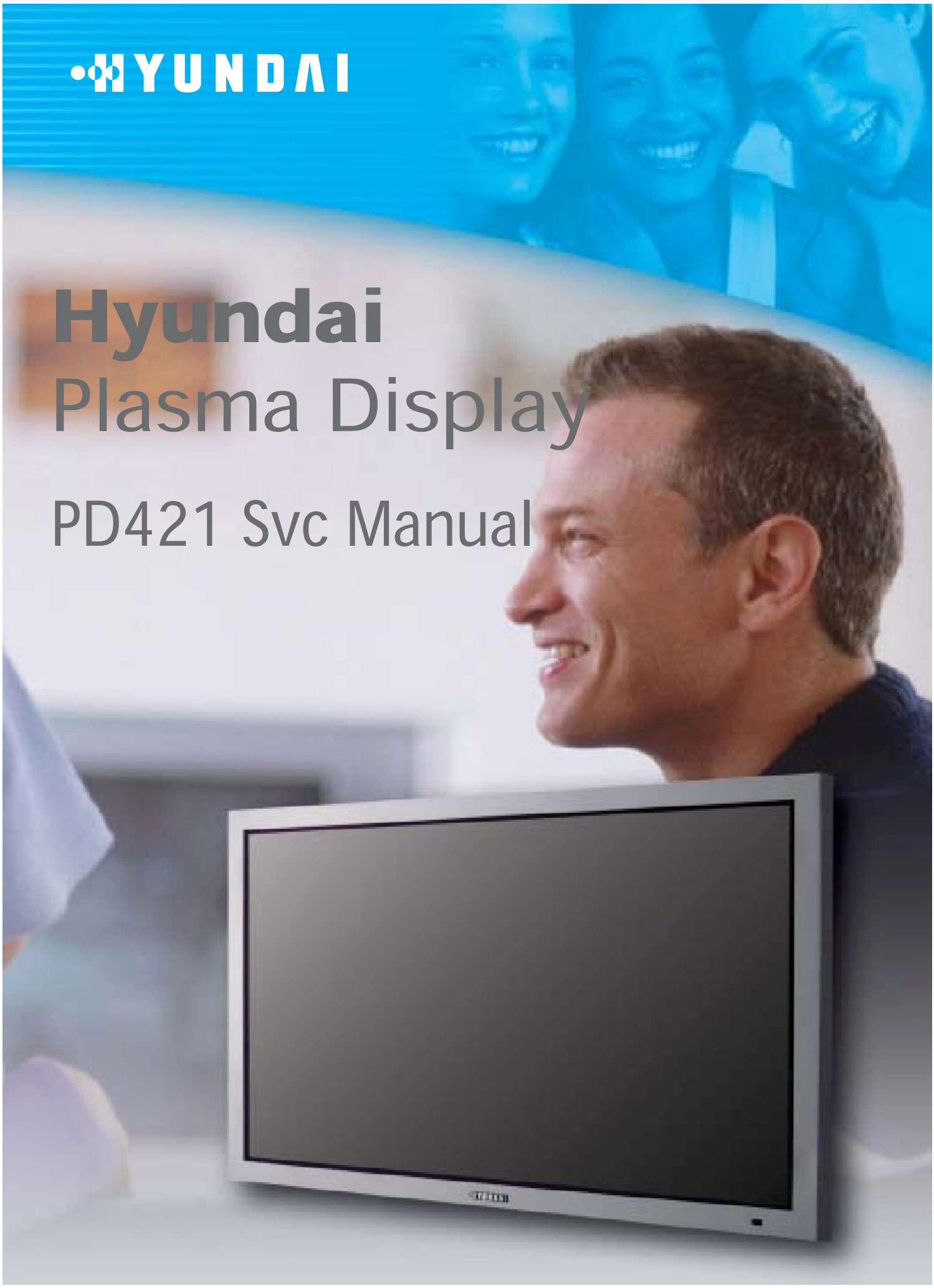
HYUNDAI

Hyundai
Plasma Display
PD421 Svc Manual



. Circuit Service Methods

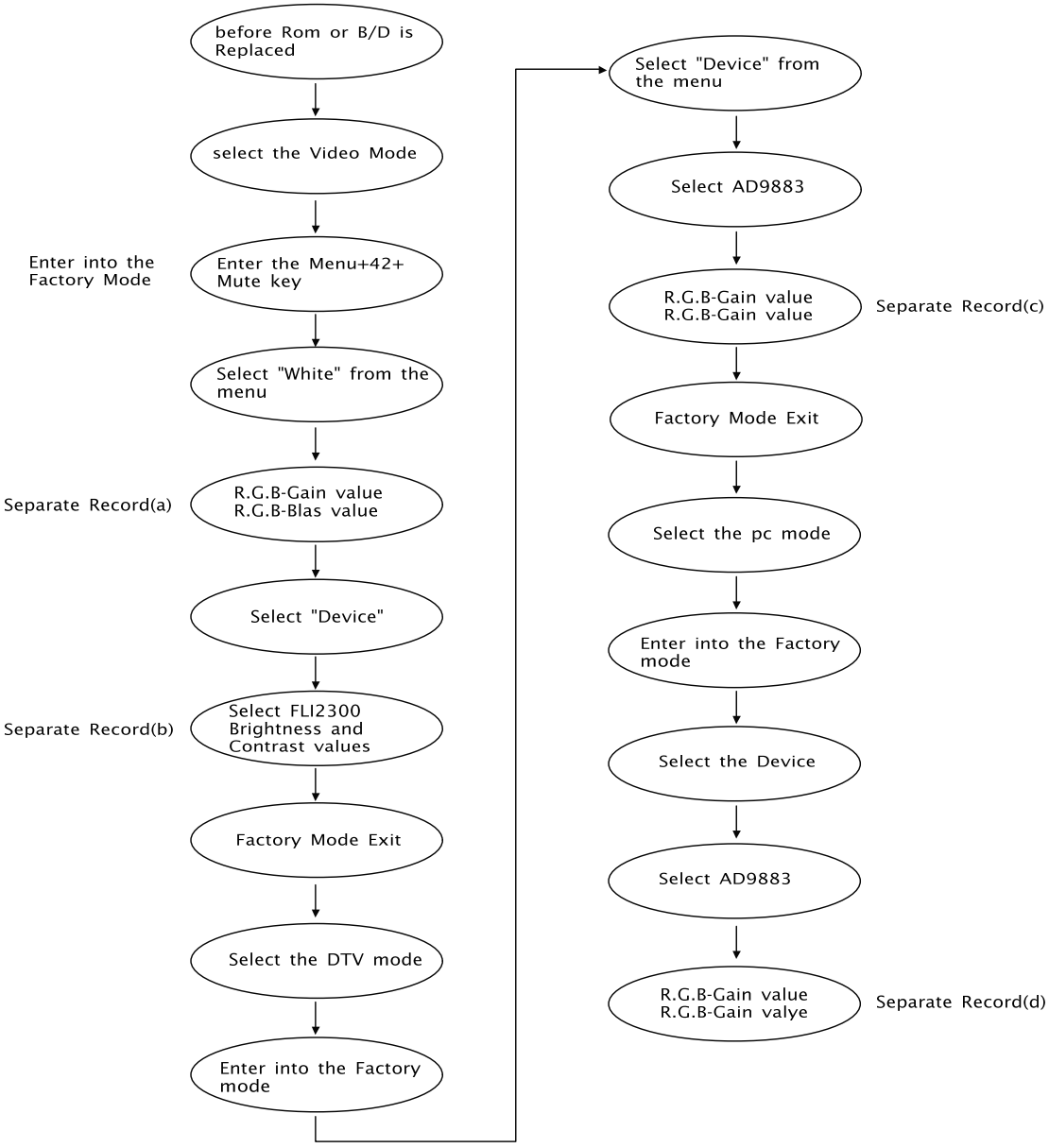
1. White Balance Adjustment

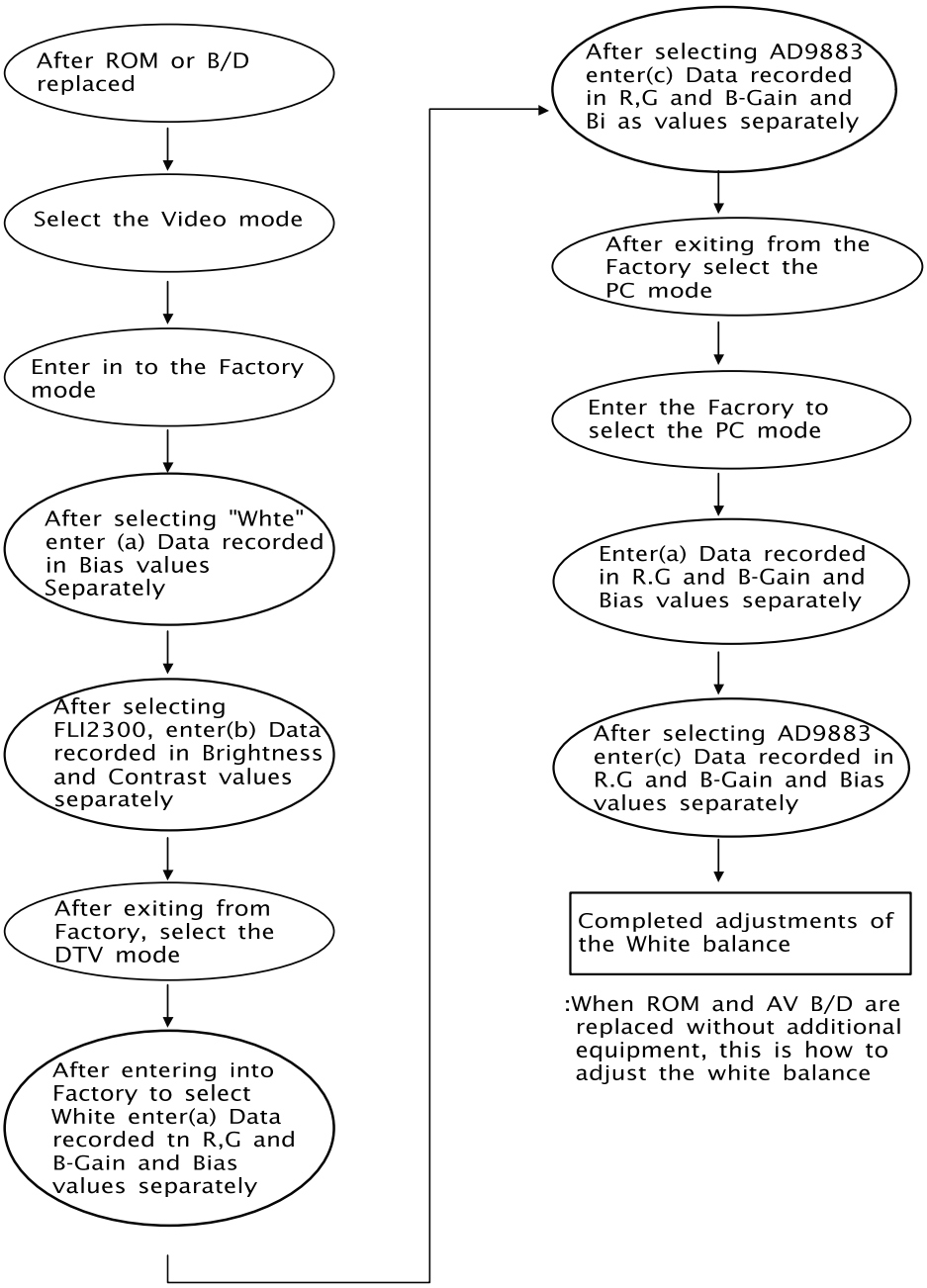
l Refer to adjustment specifications for information on making adjustments

m When white balance has to be adjusted during service

- If the module is replaced, it must be readjusted using VG-828 equipment, according to the adjustment specifications
- When making program upgrades [ROM (UM04) replacement] or replacing A/V B/D, the values stored in A/V B/D's EPROM (UM12) should be written down and re-entered into the new new Rom or A/V.Board

The method of white Balane Adjustment before ROM or B/D IS Replaced




After ROM or B/D replaced
Select the Video mode
Enter in to the Factory mode
After selecting "Whte" enter (a) Data recorded in Bias values Separately
After selecting FLI2300, enter(b) Data recorded in Brightness and Contrast values separately
After exiting from Factory, select the DTV mode
After entering into Factory to select White enter(a) Data recorded tn R,G and B-Gain and Bias values separately
After selecting AD9883 enter(c) Data recorded in R,G and B-Gain and Bi as values separately
After exiting from the Factory select the PC mode
Enter the Facrory to select the PC mode
Enter(a) Data recorded in R.G and B-Gain and Bias values separately
After selecting AD9883 enter(c) Data recorded in R.G and B-Gain and Bias values separately
Completed adjustments of the White balance

:When ROM and AV B/D are replaced without additional equipment, this is how to adjust the white balance

2. A/V Circuit BLOCK Diagram

1) PC Mode

PC inputs, R, G, B, H, and V signals, are entered through D-Sub 15pin (DSUB1). They are entered into the DTV/PC selection switch, BA7657 (UA01). When PC is selected in MCU, the signals are entered into the AD converter, AD9883 (UA02).

In AD9883, the signals are converted into 24 bits and entered into scaler ASI500.

BA7657 selects PC when pin16 is high and selects DTV when pin 16 is low.

AD9883 is controlled using the SDA/SCL line of pin 57/56.

PC input resolution is fh: 30~70k and fv: 50~85Hz, and the maximum resolution is 1080x768 at 85Hz.

If the resolution is above the specifications, an out of range message is displayed on the upper left hand corner of the screen. However, even if the resolution is within the specified range, if the input timingis different from the timing indicated on the manual, a 'not found vesa or out of range' message can be displayed. Please check the timing to identify the cause of the 'out of range' message.

PC input sync can receive H/V composite or separate, but if DPMS ON is selected in the PDP menu, DPMS cannot operate in composite and can operate only in separate sync.

The Auto Adjust function, which is used to adjust the picture position and size, should be carried out in the Windows desktop screen or full cross hatch.

The DTV signals, 480p, 720p, and 1080i, from the set-top box with a D-Sub out port, can be received through the D-Sub port and displayed in the PC mode.

DVI Mode

Signals entering through the DVI port (DV101) are converted to 24bits in the TMDS Receiver, SIL161B (UT02), and entered in scalar ASI500.

SIL161B is an output port and is activated when pin number 2 is high.

DTV signals 480p, 720p, and 1080i can be displayed through the DVI port.

However, PD421 cannot only display 60Hz DTV signals. It is unable to display 50Hz DTV signals. PC can support both 50Hz and 60Hz signals.

The resolution of DVI Mode is the same as the PC Mode.

2) DTV Mode

DTV signals are entered as Y, P b(Cb), and Pr(Cr) component signals, separated into Y, Cb, Cr, H, and V sync on (xan51AcuxA01)and entered to BA7657. If pin 16 is low, DTV signals are entered into ADC9883.
In the AD9883, like the PC signals, the DTV signals are converted to 24 bits and entered into scalar ASI500.
DTV signal is composed of 480p (50/60Hz) for SD, 720p (50/60Hz) for HD, and 1080i (50/60Hz). If the video signal, 480i component (DVD component output), is entered, the screen will not display properly. Also,
because synchronization signal is in Y singal color Data is in Cr/Cb
if the connections are incorrect, it will not operate properly

3) DVD Mode

DVD signals entered as Y, Pb, and Prcomponents are applied when entered as 480i (NT or PAL). 480p DVD signals should be entered through the DTV component port.
Y, Pb, and Pr signals entered through the DVD component port are entered into the video decoders, Main VPC3230 (UDM01) and Sub VPC3230 (UDS01), where they are converted to Y (8bits) and UV (8bits) digital signals and sent to the deinterlacer IC, FLI2310 (UFL1).
UV digital signal means Pb(Cb), and Pr(Cr) signals that have been converted to digital signals.
The video decoder, VPC3230, automatically detects NTSC and PAL/SECAM, identifies them as broadcast signals, converts the interlacer signal into the progressive signal (fh:15.7Khz-> 31Khz) in the deinterlacer IC, FLI2310 (UFL1), and sends to the scalar ASI500.
When the PD421's main screen is in PC, DVI or DTV mode, the sub-screen of the PIP or POP function is processed in the Main VIDEO DECODER (UDM01) and the MODE can be DVD, S-VHS, Video, or Scart.
PIP or POP between video modes is enabled by main video decoder (UDS01), sub video decoder (UDS01), and FIFO memory, MS81V04160 (UFM01). If the main screen is DVD, then the sub-screen will be S-VHS, Video, or Scart.
Please refer to the table in the back for more information on PIP or POP.

4) S-Video

S-Video signals are entered as Y/C signals, which is composed of Luminance

color signals. The NTSC and PAL/SECAM are automatically detected by the video decoders, main VPC3230 and sub VPC3230, and converted to Y (8bits) and UV (8bits) and sent to the deinterlacer IC, FLI2310, as 16bit digital signal.

S-Video input and composite video input share a single audio jack. Therefore, while the pictures for the two inputs can be viewed at the same time, only one of the sounds can be heard. PIP/POP operations are the same as described for the DVD mode.

5) Video

Video signal is a composite signal that combines the Luminance(Y) and color (CHROMA).

It is entered through the main VPC3230 and sub VPC3230 when selected in the input selection switch, TA8851 (UMX01).

If the signal is NTSC, it is first entered into the 3D Comb Filter (filter that separates the composite to Y/C signal), UPD 64083 (UCF 01) and separated into Luminance signal Y and color signal, C. The separated signals then enter the mux switch, TA8851, sent to TA8851 pin44 LUMA IN and pin43 CROMA IN, and finally sent to Main VPC3230.

When the video input is displayed on the main screen, it passes through the 3D comb filter, but if it is displayed on the sub-screen (when using PIP or POP), the video input does not pass through the 3D comb filter and is displayed using the composite signal.

PAL/SECAM signal cannot be processed by the 3D comb filter. It is sent as composite signal to the main VPC3230 and sub VPC3230.

If the signal is NTSC, the video input switch, BF 7654 (UDM02), which is located in front of the main VPC3230, select the 3D Comb-Y to send the signal as a Y signal to the VPC 3230. If the signal is Pal, it selects CVBS to send the signal as a composite signal to the VPC3230.

Signals entered into VPC3230 are converted to 16bit digital signal (Y (8bits) and UV (8bits)) and sent to the scalar through the deinterlacer IC, FLI2310.

6) Scart Mode

Scart only supports CVBS signals, which are processed in the same way as video signals. The RF signal is not supported, and therefore, the Scart pin8 ID signal is ignored.

7) PIP/POP Support Mode Map

Main \ Sub	PC	DTV	DVD	S-VHS	Video	Scart	DVI
PC	X	X	O	O	O	O	X
DTV	X	X	O	O	O	O	X
DVD	O	O	X	O	O	O	O
S-VHS	O	O	O	X	O	O	O
Video	O	O	O	O	X	O	O
Scart	O	O	O	O	O	X	O
DVI	X	X	O	O	O	O	X

X: Not supported, O: Supported

Note: When displaying NTSC or PAL signals to PIP or POP, if the signals are displayed as Main: NTSC, Sub: PAL or in reverse, the picture can be seen, but the size scaling for the sub-screen will not display properly. This is because the signal is meant for the main screen. Main screen uses 50Hz PAL or 60Hz NTSC and sub screen uses 60Hz NTSC or 50Hz.

8) Scaler Output

Scaler output signals, R, G, and B (each 8bits), are outputted as 24bit TTL signal, converted into LVDS signal in the LVDS converter, DS90C385 (ULV01), and sent to the logic B/D in the PDP module. Output timing:

fh : 29.1Khz
fv : PAL 50Hz NTSC 60Hz
DCLK : about 27Mhz

9) Audio part

Audio inputport for each mode:

Input	Port	Remark
PC/DVI	RCA L/R 1EA	Shared
DTV	RCA L/R 1EA	
DVD	RCA L/R 1EA	
CVBS/S-Video	RCA L/R 1EA	Shared
Scart	Scart Jack L/R	

Audio input signal for PC/DVI, DTV, and DVD modes is entered into the audio processor IC, MSP3450G, and audio input signal for VIDEO/S-VIDEO, and SCART modes is first selected in MUX 8851 and entered into the audio processor.

As in other chips, the audio processor (MSP3450G) uses the SCL and SDA line to control volume, and left/right balance and mono/stereo.

The L/R audio signal sent by MSP3450 is amplified in the amplifier, TA2024 (UAU1) and sent to the speaker.

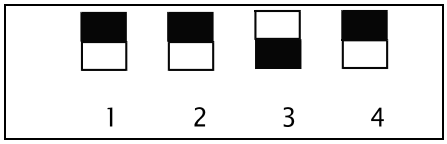
TA2024B support 10W(based on impedance 8Y) of output for each L/R.

3. Trouble shooting

1) Diagnosing defective module

If the power does not come on or if the module operates abnormally, check module defect. To do this, remove the rear cover and A/V B/D to reveal the module's logic B/D. The following figure represents the s/w on the logic B/D.

SW 2001



Signal	1	2	3	4	Remark
External	up	up	down	up	Forwarding Criteria
Internal	up	down	up	down	

If the switch is set to internal signals, it will operate without external signals, but the screen will be displayed in full white.

Therefore the module operation can be checked without the A/V board.

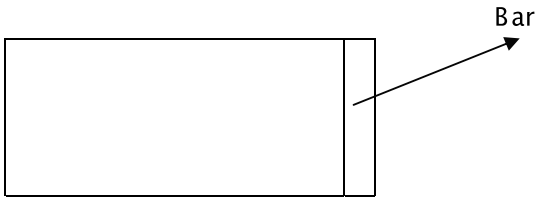
Here, be aware that the pin 8 and pin 9 of the power B/D's CN802(11p), which is located above the module's logic B/D, must be shorted and the A/C power supplied in order for the module to operate normally. Pin 8 is marked as PS-ON below the connector (CN802).

If module itself is tested and it does not power on or the picture is abnormal, the module is defective.

When reconnecting the A/V B/D, make sure to change the switch to external signals.

- The most common module defect is the appearance of a black or bright vertical line.

-



This occurs when the FPC wire, which connects the address line below the module, is damaged. Because the wire is on the bottom, it can be easily damaged when the module is lifted and assembled or from external shock. Use caution when handling the module and use the handle on the bottom of the module to lift or move.

If the vertical bar appears at the same location for all modes, the FPC wire is damaged.

FPC wire cannot be replaced. The entire module needs to be replaced.

- If the module does not power on, it is mostly likely due to an open fuse on the power B/D. Check the black and round fuse on the power B/D.

2) Diagnosis by Problem Type

- Power comes on, but the picture does display

  Check the AV B/D's communication lines, SDL and SDA lines.

  ICs controlled by the SDA and SCL line are ADC9883, FLI2310, MSP3450G, VPC3230, 3D comb filter, and TA8851. If after powering on, the SDA and SCL line's Vp-p is less than 4V and checks below 2.5V, the communication line is loaded at some point. Open and check each IC's communication line.

- Can also occur when the connection between the graphic B/D and video B/D is bad.

- If the picture turns off or the volume is muted while viewing through the set-top box, please check the status of the set-top box first.

- For abnormal picture when using PIP/POP function, refer to the section on Video Mode in the manual

- If the OSD screen cracks or displays abnormally:

  May be caused by bad connection between the graphic B/D's scaler and SDRAM, K4S643232C (UFB01, UFB02). Use the cleaner to clean the around the scaler and the UFB01/02.

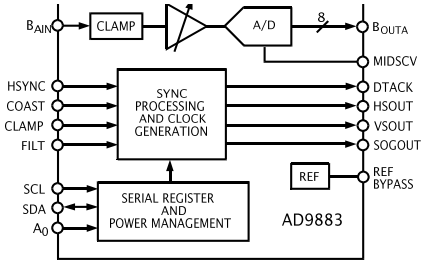
  OSD is processed by the scaler (ASI 500).

- If the power is on and the input signals and connections are normal, but the picture does not display:

Critical Parts Specification

AD9883

Sync Detect to "Hot" Plugging
Midscale Clamping
Power-Down Mode
Low Power : 500mW tYPICAL
Composite Sync Applications Require an External Coast



GENERAL DESCRIPTION

The AD9883 is a complete 8-bit, 110 MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 110 MSPS encode rate capability and full-power analog bandwidth of 300 MHz supports resolutions up to SXGA (1280X1024 at 60Hz)

The AD9883 includes a 110 MHz triple ADC with internal 1.25 V reference, a PLL, and programmable gain, offset, and clamp control. The user provides only a 3.3 V power supply, analog input, and HSYNC and COAST signals. Three-state CMOS outputs may be powered from 2.5 V to 3.3 V.

The AD9883's on-chip PLL generates a pixel clock from HSYNC and COAST inputs. Pixel clock output frequencies range from 12 MHz to 110 MHz. PLL clock jitter is 500 ps p-p typical at 10 MSPS. When the COAST signal is presented, the PLL maintains its output frequency in the absence of HSYNC. A sampling phase adjustment is provided. Data, HSYNC and Clock output phase relationships are maintained. The AD9883 also offers full sync processing for composite sync and sync-on-green applications.

A clamp signal is generated internally or may be provided by the user through the CLAMP input pin. This interface is fully programmable via a two-wire serial interface.

Fabricated in an advanced CMOS process, the AD9883 is provided in a space-saving 80-lead LQFP surface mount plastic package and is specified over the 0 C to 70 C temperature range.

AD9883–SPECIFICATIONS

Analog Interface (V_D = 3.3 V, V_{DD} = 3.3 V, ADC Clock = Maximum Conversion Rate)

Parameter	Temp	Test Level	AD9883KST-110 Min	Typ	Max	Unit
RESOLUTION				8		Bits
DC ACCURACY						
Differential Nonlinearity	25°C	I		0.5	+1.25/–1.0	LSB
	Full	VI			+1.35/–1.0	LSB
Integral Nonlinearity	25°C	I		0.5	1.85	LSB
	Full	VI			2.0	LSB
No Missing Codes	Full	VI		Guaranteed		
ANALOG INPUT						
Input Voltage Range						
Minimum	Full	VI			0.5	V p-p
Maximum	Full	VI	1.0			V p-p
Gain Tempco	25°C	V		100		ppm/°C
Input Bias Current	25°C	IV			1	µA
	Full	IV			1	µA
Input Offset Voltage	Full	VI		7	50	mV
Input Full-Scale Matching	Full	VI			6.0	% FS
Offset Adjustment Range	Full	VI	46	49	52	% FS
REFERENCE OUTPUT						
Output Voltage	Full	VI	1.20	1.25	1.32	V
Temperature Coefficient	Full	V		50		ppm/°C
SWITCHING PERFORMANCE						
Maximum Conversion Rate	Full	VI	110			MSPS
Minimum Conversion Rate	Full	IV			10	MSPS
Data to Clock Skew	Full	IV	–0.5		+2.0	ns
t_{BUFF}	Full	VI	4.7			µs
t_{STAH}	Full	VI	4.0			µs
t_{DHO}	Full	VI	0			µs
t_{DAL}	Full	VI	4.7			µs
t_{DAH}	Full	VI	4.0			µs
t_{DSU}	Full	VI	250			µs
t_{STASU}	Full	VI	4.7			µs
t_{STOSU}	Full	VI	4.0			µs
HSYNC Input Frequency	Full	IV	15		110	kHz
Maximum PLL Clock Rate	Full	VI	110			MHz
Minimum PLL Clock Rate	Full	IV			12	MHz
PLL Jitter	25°C	IV		400	700[1]	ps p-p
	Full	IV			1000[1]	ps p-p
Sampling Phase Tempco	Full	IV		15		ps/°C
DIGITAL INPUTS						
Input Voltage, High (V_{IH})	Full	VI	2.5			V
Input Voltage, Low (V_{IL})	Full	VI			0.8	V
Input Voltage, High (V_{IH})	Full	V			–1.0	µA
Input Voltage, Low (V_{IL})	Full	V			1.0	µA
Input Capacitance	25°C	V		3		pF
DIGITAL OUTPUTS						
Output Voltage, High (V_{OH})	Full	VI	V_D – 0.1			V
Output Voltage, Low (V_{OL})	Full	VI			0.1	V
Duty Cycle DATACK	Full	IV	45	50	55	%
Output Coding				Binary		

Parameter	Temp	Test Level	AD9883KST-110 Min	Typ	Max	Unit
POWER SUPPLY						
V_D Supply Voltage	Full	IV	3.0	3.3	3.6	V
V_{DD} Supply Voltage	Full	IV	2.2	3.3	3.6	V
P_{VD} Supply Voltage	Full	IV	3.0	3.3	3.6	V
I_D Supply Current (V_D)	25 C	V		132		mA
I_{DD} Supply Current (V_{DD})[2]	25 C	V		19		mA
IP_{VD} Supply Current (P_{VD})	25 C	V		8		mA
Total Power Dissipation	Full	VI		525	650	mW
Power-Down Supply Current	Full	VI		5	10	mA
Power-Down Dissipation	Full	VI		16.5	33	mW
DYNAMIC PERFORMANCE						
Analog Bandwidth, Full Power	25 C	V		300		MHz
Transient Response	25 C	V		2		ns
Overvoltage Recovery Time	25 C	V		1.5		ns
Signal-to-Noise Ratio (SNR)	25 C	V		44		dB
(Without Harmonics)	Full	V		43		dB
f_{IN} = 40.7 MHz						
Crosstalk	Full	V		55		dBc
THERMAL CHARACTERISTICS						
$_{JC}$ Junction-to-Case Thermal Resistance		V		16		C/W
$_{JA}$ Junction-to-Ambient Thermal Resistance		V		35		C/W

NOTES
[1]VCO Range = 10, Charge Pump Current = 110, PLL Divider = 1693.
[2]DATACK Load = 15 pF, Data Load = 5 pF.

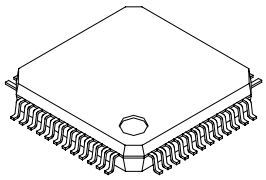
Specifications subject to change without notice.

CXA2151Q

Description

The CXA2151Q is a bipolar IC developed for multi scan TVs, and incorporates a four system video switch (including HV sync signal processing) and a YCbCr output matrix circuit.

48 pin QFP (Plastic)



Features

- Supports the ^{2}IC bus
- Supports multi scan
- Four system video switch (of which two systems support D3 pins)
- Matrix circuit
- Each YCbCr output can be switched between 0dB, 6dB (gain adjustable) and mute.
- Sync signal automatic identification circuit (with fixed mode)
- Sync separation circuit (supports HD)
- HD Tri-level sync identification circuit
- Sync signal frequency counter (both H and V)
- Dummy sync output

Applications

Multi scan TVs

Structure

Bipolar silicon monolithic IC

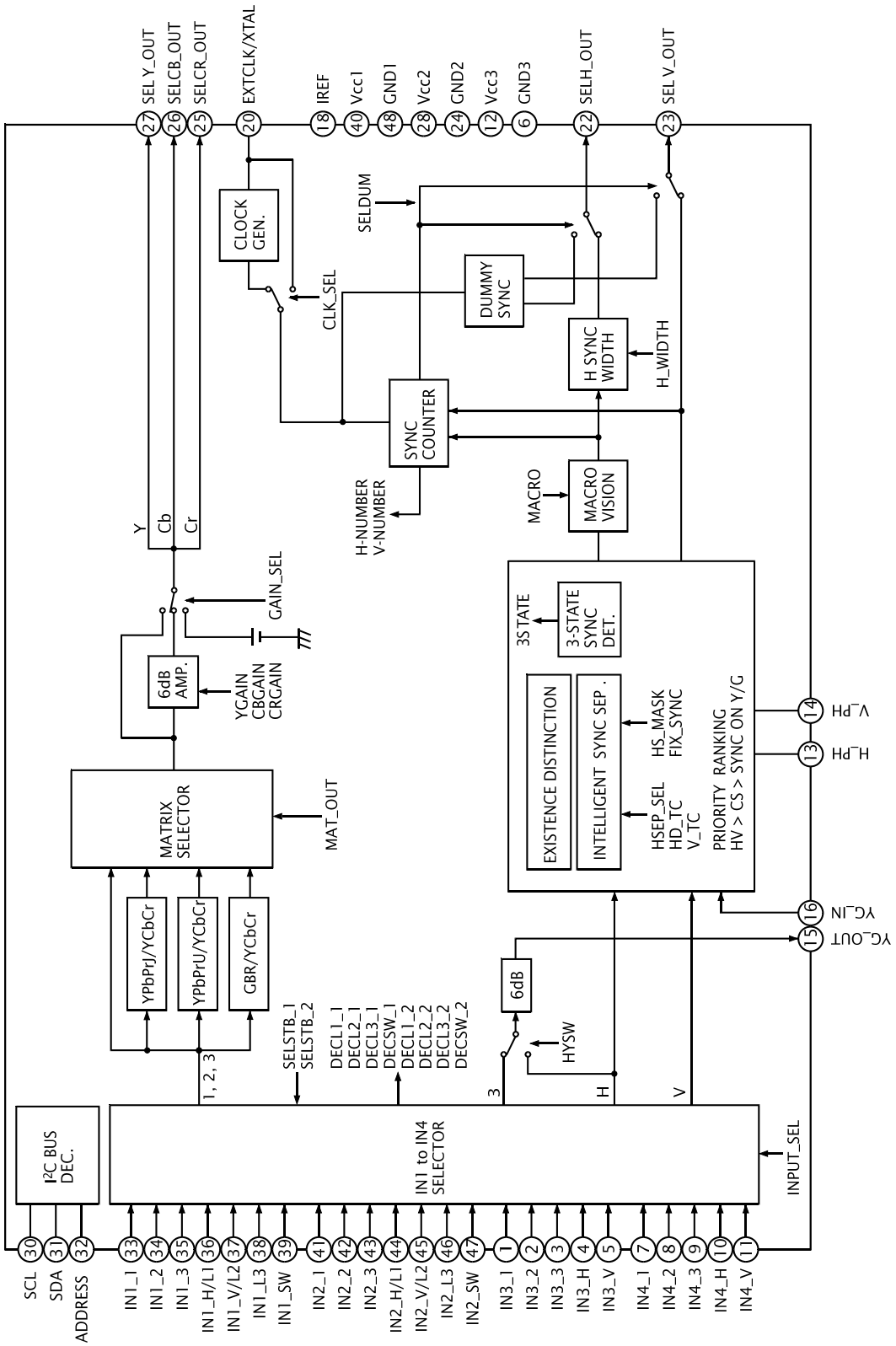
Absolute Maximum Ratings (Ta = 25°C, GND1, 2, 3 = 0V)

▪ Supply voltage	V_{CC}1, 2, 3	−0.3 to +5.5	V
▪ Operating temperature	Topr	−20 to +75	°C
▪ Storage temperature	Tstg	−65 to +150	°C
▪ Allowable power dissipation	P_D	1400	mW
(when mounted on a 50mm 50mm board)			
▪ Voltage at each pin	−0.3 to V_{CC}1, 2, 3 + 0.3		V

Recommended Operating Conditions

Supply voltage	V_{CC}1, 2, 3	5 ± 0.25	V

Block Diagram



DS90C385

General Description

The DS90C385 transmitter converts 28 bits of LVCMOS/LVTTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 85 MHz, 24 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 595 Mbps per LVDS data channel. Using a 85 MHz clock, the data throughput is 297.5 Mbytes/sec. Also available is the DS90C365 that converts 21 bits of LVCMOS/LVTTL data into three LVDS (Low Voltage Differential Signaling) data streams. Both transmitters can be programmed for Rising edge strobe or Falling edge strobe through a dedicated pin. A Rising edge or Falling edge strobe transmitter will interoperate with a Falling edge strobe Receiver (DS90CF386/DS90CF366) without any translation logic.

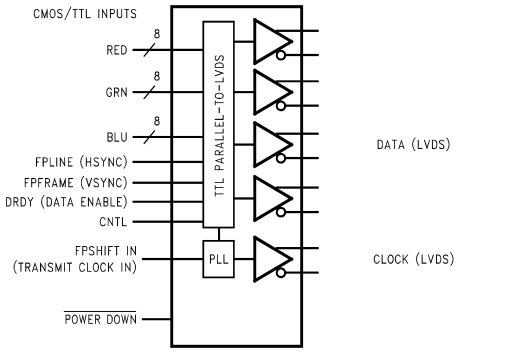
The DS90C385 is also offered in a 64 ball, 0.8mm fine pitch ball grid array (FBGA) package which provides a 44 % reduction in PCB footprint compared to the TSSOP package. This chipset is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces.

Features

- 20 to 85 MHz shift clock support
- Best±in±Class Set & Hold Times on TxINPUTs
- Tx power consumption <130 mW (typ) @85MHz Grayscale
- Tx Power-down mode <200 W (max)
- Supports VGA, SVGA, XGA and Single/Dual Pixel SXGA.
- Narrow bus reduces cable size and cost
- Up to 2.38 Gbps throughput
- Up to 297.5 Megabytes/sec bandwidth
- 345 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Compatible with TIA/EIA-644 LVDS standard
- Low profile 56-lead or 48-lead TSSOP package
- DS90C385 also available in a 64 ball, 0.8mm fine pitch ball grid array (FBGA) package

Block Diagrams

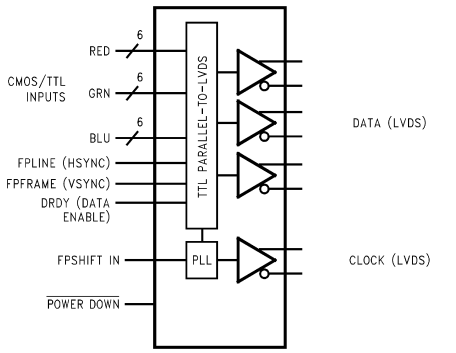
DS90C385



DS100868-1

Order Number DS90C385MTD or DS90C385SLC
See NS Package Number MTD56 or SLC64A

DS90C365



DS100868-29

Order Number DS90C365MTD
See NS Package Number MTD48

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.3V to +4V
CMOS/TTL Input Voltage	-0.5V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	-0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150°C
Storage Temperature	-65 C to +150°C
Lead Temperature (Soldering, 4 sec)	+260°C
Solder reflow Temperature (20 sec for FBGA)	+220°C
Maximum Package Power Dissipation Capacity @ 25°C	
MTD56 (TSSOP) Package: DS90C385MTD	1.63W
MTD48 (TSSOP) Package: DS90C365MTD	1.98W
SLC64 (FBGA) Package: DS90C385SLC	2.0W
Package Derating: DS90C385MTD	12.5mW/ C above +25°C
Package Derating: DS90C365MTD	16 mW/ C above +25°C
DS90C385SLC	10.2mW/ C above +25°C
ESD Rating	
(HBM, 1.5kW, 100pF)	> 7 kV
(EIAJ, 0W, 200 pF)	> 500V
Latch Up Tolerance @ 25°C	> +/-300mA

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	-10	+25	+70	°C
Supply Noise Voltage (V_{CC})			100	mV_{PP}
TxCLKIN frequency	20		85	MHz

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVCMOS/LVTTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = -18 mA			-0.79	-1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}			+1.8	+10	A
		V_{IN} = GND		-10	0		A
LVDS DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100W		250	345	450	mV
DV_{OD}	Change in V_{OD} between complimentary output states					35	mV
V_{OS}	Offset Voltage (Note 4)			1.125	1.25	1.375	V
DV_{OS}	Change in V_{OS} between complimentary output states					35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100W			-3.5	-5	mA
I_{OZ}	Output TRI-STATE Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0 V or V_{CC}			+/-1	+/-10	A
TRANSMITTER SUPPLY CURRENT							
ICCTW	Transmitter Supply Current Worst Case DS90C385	R_L = 100W, C_L = 5 pF, Worst Case Pattern *(Figures 1, 4)*	f = 32.5 MHz		31	45	mA
			f = 40 MHz		32	50	mA
			f = 65 MHz		37	55	mA
			f = 85 MHz		42	60	mA
ICCTG	Transmitter Supply Current 16 Grayscale DS90C385	R_L = 100W, C_L = 5 pF, 16 Grayscale Pattern *(Figures 2, 4)*	f = 32.5 MHz		29	38	mA
			f = 40 MHz		30	40	mA
			f = 65 MHz		35	45	mA
			f = 85 MHz		39	50	mA
ICCTW	Transmitter Supply Current Worst Case DS90C365	R_L = 100W, C_L = 5 pF, Worst Case Pattern *(Figures 1, 4)*	f = 32.5 MHz		28	42	mA
			f = 40 MHz		29	47	mA
			f = 65 MHz		34	52	mA
			f = 85 MHz		39	57	mA

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
ICCTG	Transmitter Supply Current 16 Grayscale DS90C365	R_L = 100W, C_L = 5 pF, 16 Grayscale Pattern *(Figures 3, 4)*	f = 32.5 MHz		26	35	mA
			f = 40 MHz		27	37	mA
			f = 65 MHz		32	42	mA
			f = 85 MHz		36	47	mA
ICCTZ	Transmitter Supply Current Power Down	$\overline{\text{Power Down}}$ = Low Driver Outputs in TRI-STATE under Power Down Mode			10	55	A

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 3.3V and T_A = +25C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: V_{OS} previously referred as V_{CM}.

Recommended Transmitter Input Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
TCIT	TxCLK IN Transition Time *(Figure 6)*	1.0		6.0	ns
TCIP	TxCLK IN Period *(Figure 7)*	11.76	T	50	ns
TCIH	TxCLK IN High Time *(Figure 7)*	0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 7)*	0.35T	0.5T	0.65T	ns
TXIT	TxIN Transition Time	1.5		6.0	ns

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 5)*			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 5)*			0.75	1.5	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 *(Figures 13, 14)* (Note 5)	f = 40 MHz	-0.25	0	0.25	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		3.32	3.57	3.82	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		6.89	7.14	7.39	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		10.46	10.71	10.96	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		14.04	14.29	14.54	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		17.61	17.86	18.11	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		21.18	21.43	21.68	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 *(Figures 13, 14)* (Note 5)	f = 65 MHz	-0.20	0	0.20	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		2.00	2.20	2.40	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		4.20	4.40	4.60	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		6.39	6.59	6.79	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		8.59	8.79	8.99	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		10.79	10.99	11.19	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		12.99	13.19	13.39	ns

Transmitter Switching Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
TPPos0	Transmitter Output Pulse Position for Bit 0 *(Figures 13, 14)* (Note 5)	f = 85 MHz	-0.20	0	0.20	ns
TPPos1	Transmitter Output Pulse Position for Bit 1		1.48	1.68	1.88	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		3.16	3.36	3.56	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		4.84	5.04	5.24	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		6.52	6.72	6.92	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		8.20	8.40	8.60	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		9.88	10.08	10.28	ns
TSTC	TxIN Setup to TxCLK IN *(Figure 7)*		2.5			ns
THTC	TxIN Hold to TxCLK IN *(Figure 7)*		0			ns
TCCD	TxCLK IN to TxCLK OUT Delay *(Figure 8)*	T_A = 25 C, V_{CC} = 3.3V	3.8		6.3	ns
	TxCLK IN to TxCLK OUT Delay *(Figure 8)*		2.8		7.1	ns
TJCC	Transmitter Jitter Cycle-to-Cycle *(Figures 15, 16)* (Note 6)	f = 85 MHz		110	150	ps
		f = 65 MHz		210	230	ps
		f = 40 MHz		350	370	ps
TPLLS	Transmitter Phase Lock Loop Set *(Figure 9)*				10	ms
TPDD	Transmitter Power Down Delay *(Figure 12)*				100	ns

Note 5: The Minimum and Maximum Limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. This parameter is functionality tested only on Automatic Test Equipment (ATE).

Note 6: The limits are based on bench characterization of the device's jitter response over the power supply voltage range. Output clock jitter is measured with a cycle-to-cycle jitter of +/- .3ns applied to the input clock signal while data inputs are switching (See Figures 15 and 16). A jitter event of 3ns, represents worse case jump in the clock edge from most graphics controller VGA chips currently available. This parameter is used when calculating system margin as described in AN-1059.

AC Timing Diagrams

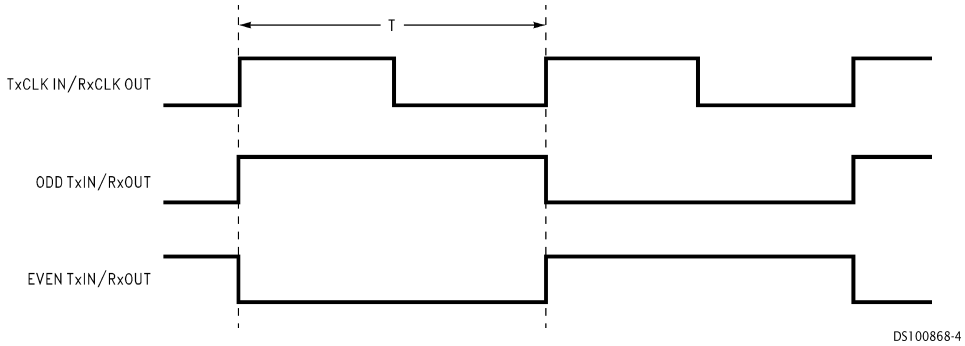


FIGURE 1. "Worst Case" Test Pattern (Note 7)

P89C51RD2BA

DESCRIPTION

The P89C51RB2/RC2/RD2 device contains a non-volatile 16kB/32kB/64kB Flash program memory that is both parallel programmable and serial In-System and In-Application Programmable. In-System Programming (ISP) allows the user to download new code while the microcontroller sits in the application. In-Application Programming (IAP) means that the microcontroller fetches new program code and reprograms itself while in the system. This allows for remote programming over a modem link. A default serial loader (boot loader) program in ROM allows serial In-System programming of the Flash memory via the UART without the need for a loader in the Flash code. For In-Application Programming, the user program erases and reprograms the Flash memory by use of standard routines contained in ROM.

This device executes one machine cycle in 6 clock cycles, hence providing twice the speed of a conventional 80C51. An OTP configuration bit lets the user select conventional 12 clock timing if desired.

This device is a Single-Chip 8-Bit Microcontroller manufactured in advanced CMOS process and is a derivative of the 80C51 microcontroller family. The instruction set is 100% compatible with the 80C51 instruction set.

The device also has four 8-bit I/O ports, three 16-bit timer/event counters, a multi-source, four-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits.

The added features of the P89C51RB2/RC2/RD2 makes it a powerful microcontroller for applications that require pulse width modulation, high-speed I/O and up/down counting capabilities such as motor control.

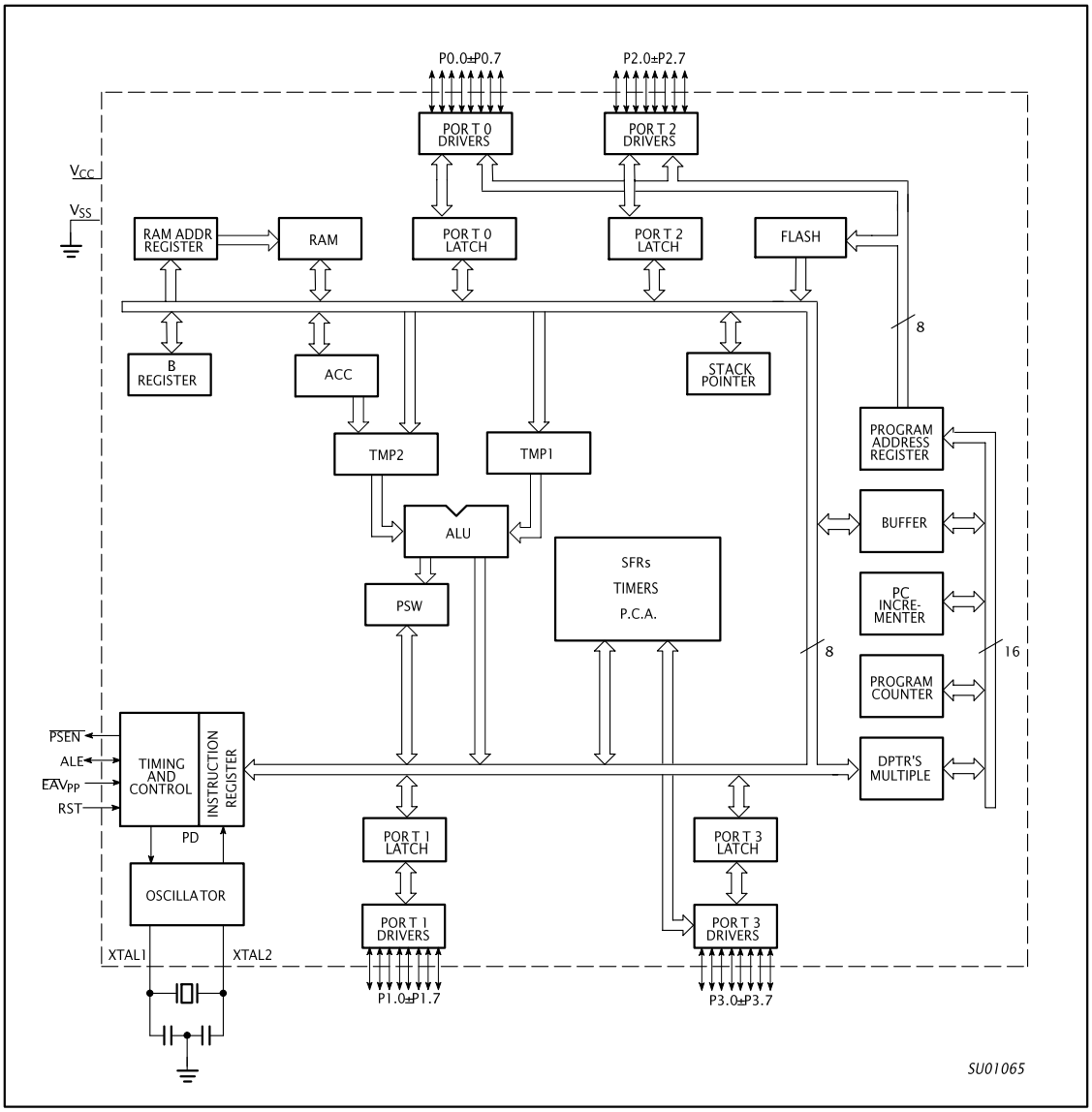
FEATURES

- 80C51 Central Processing Unit
- On-chip Flash Program Memory with In-System Programming (ISP) and In-Application Programming (IAP) capability
- Boot ROM contains low level Flash programming routines for downloading via the UART
- Can be programmed by the end-user application (IAP)
- 6 clocks per machine cycle operation (standard)
- 12 clocks per machine cycle operation (optional)
- Speed up to 20 MHz with 6 clock cycles per machine cycle (40 MHz equivalent performance); up to 33 MHz with 12 clocks per machine cycle
- Fully static operation
- RAM expandable externally to 64 kB
- 4 level priority interrupt
- 7 interrupt sources
- Four 8-bit I/O ports
- Full-duplex enhanced UART
  - ± Framing error detection
  - ± Automatic address recognition
- Power control modes
  - ± Clock can be stopped and resumed
  - ± Idle mode
  - ± Power down mode
- Programmable clock out
- Second DPTR register
- Asynchronous port reset
- Low EMI (inhibit ALE)
- Programmable Counter Array (PCA)
  - ± PWM
  - ± Capture/compare

ORDERING INFORMATION

	PHILIPS (EXCEPT NORTH AMERICA) PART ORDER NUMBER PART MARKING	PHILIPS NORTH AMERICA PART ORDER NUMBER	MEMORY		TEMPERATURE RANGE (°C) AND PACKAGE	VOLTAGE RANGE	FREQUENCY (MHz)		DWG #
			FLASH	RAM			6 CLOCK MODE	12 CLOCK MODE	
1	P89C51RB2HBA	P89C51RB2BA	16 kB	512 B	0 to +70, PLCC	4.5±5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
2	P89C51RB2HBBD	P89C51RB2BBD	16 kB	512 B	0 to +70, LQFP	4.5±5.5 V	0 to 20 MHz	0 to 33 MHz	SOT389-1
3	P89C51RC2HBP	P89C51RC2BP	32 kB	512 B	0 to +70, PDIP	4.5±5.5 V	0 to 20 MHz	0 to 33 MHz	SOT129-1
4	P89C51RC2HBA	P89C51RC2BA	32 kB	512 B	0 to +70, PLCC	4.5±5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
5	P89C51RC2HFA	P89C51RC2FA	32 kB	512 B	±40 to +85, PLCC	4.5±5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
6	P89C51RC2HBBD	P89C51RC2BBD	32 kB	512 B	0 to +70, LQFP	4.5±5.5 V	0 to 20 MHz	0 to 33 MHz	SOT389-1
7	P89C51RC2HFBD	P89C51RC2FBD	32 kB	512 B	±40 to +85, LQFP	4.5±5.5 V	0 to 20 MHz	0 to 33 MHz	SOT389-1
8	P89C51RD2HBP	P89C51RD2BP	64 kB	1 kB	0 to +70, PDIP	4.5±5.5 V	0 to 20 MHz	0 to 33 MHz	SOT129-1
9	P89C51RD2HBA	P89C51RD2BA	64 kB	1 kB	0 to +70, PLCC	4.5±5.5 V	0 to 20 MHz	0 to 33 MHz	SOT187-2
10	P89C51RD2HBBD	P89C51RD2BBD	64 kB	1 kB	0 to +70, LQFP	4.5±5.5 V	0 to 20 MHz	0 to 33 MHz	SOT389-1

BLOCK DIAGRAM



S2310

DESCRIPTION

The s2300 is a highly integrated digital video format converter for DTV and DVD applications using patented deinterlacing and post processing algorithms from Faroudja Laboratories, coupled with highly flexible scaling, a wide variety of aspect ratio conversions, and other special video enhancing features to produce the highest quality image.

INPUTS –

- Input all industry standard and non-standard video resolutions, including 480i (NTSC), 576i (PAL/SECAM), 480p, 720p, 1080i, and VGA to SXGA
- Digital input, 8-bit Y/Cr/Cb (ITU-R BT656), 8-bit Y/Pr/Pb, 16-bit Y Cr/Cb (ITU-R BT601), 24-bit RGB, YCrCb, YPrPb
- Input pixel rate up to 75MHz maximum

OUTPUTS –

- Output resolutions include 480p, 576i, 576p, 720p, 1080i, 1080p, and VGA to SXGA
- Interlaced or Progressive output
- Output can be either analog YUV/RGB (through the integrated 10-bit DAC), or digital 24-bit RGB, YCrCb, YPrPb (4:4:4), or digital 16/20-bit Y Cr/Cb (4:2:2)
- Output pixel rate up to 150MHz maximum

FORMATS –

- Input color manipulation matrix supports all color spaces: RGB, YPrPb, 4:4:4 YCrCb, 4:2:2 YCr/Cb, ITU-R BT656, ITU-R BT601
- Output supports analog RGB, YPrPb, YCrCb, and digital RGB, YPrPb, 4:4:4 YCrCb, 4:2:2 YCr/Cb

FRONT END PROCESSING –

- Motion Adaptive Noise Reduction - Improves picture quality for off-air material.
- Cross Color Suppressor (CCS) - Removes cross color artifacts in composite video signals due to poor Y/C separation in standard 2D video decoders, eliminating the need for expensive 3D video decoders.

DEINTERLACING –

- Per-pixel Motion Adaptive Deinterlacing
- Patented FilmMode Processing - Used for proper de-interlacing of 3:2 and 2:2 pulldown material.
- Edit Correction - Film content is continuously monitored for any break in sequence caused by “bad edits” and quickly compensates for the most effective reduction in artifacts.
- DCDi™ - Video is analyzed on a single pixel granularity to detect presence or absence of angled lines and edges, which are then processed to produce a smooth & natural looking image without visible artifacts or “jaggies”.

SCALING –

- High Quality Fully Programmable Two Dimensional Scaler
- Aspect Ratio Conversion for “Anamorphic” or “Panoramic” (non-linear)
- Display 4:3 images on 16:9 displays and vice versa, including Letterbox to Fullscreen, Pillarbox, and Subtitle Display Modes

TrueLife™ ENHANCER –

Two dimensional, non-linear, luma & chroma video enhancer brings out details in the picture, producing a more life-like image.

MEMORY –

- 32-bit wide SDRAM (i.e. one 2Mx32bit, or two 1Mx16bit), up to 166MHz operation

FRC –

- Tearless Frame Rate Conversion, 50/60/72/75/100/120 Hz

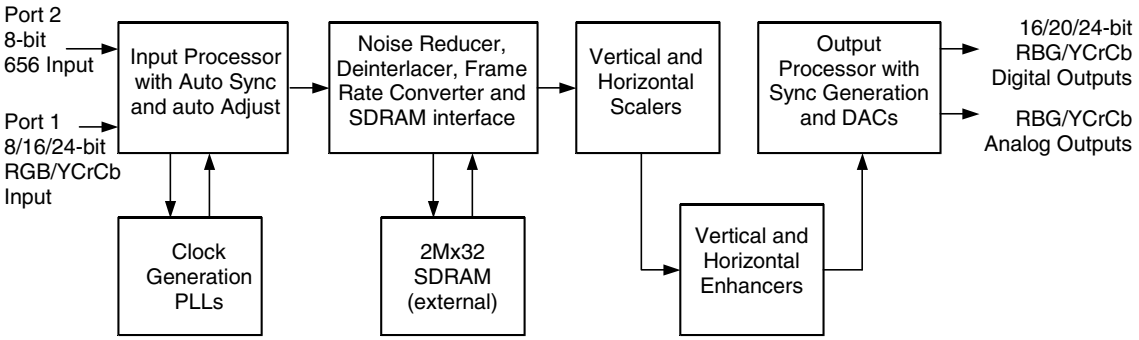
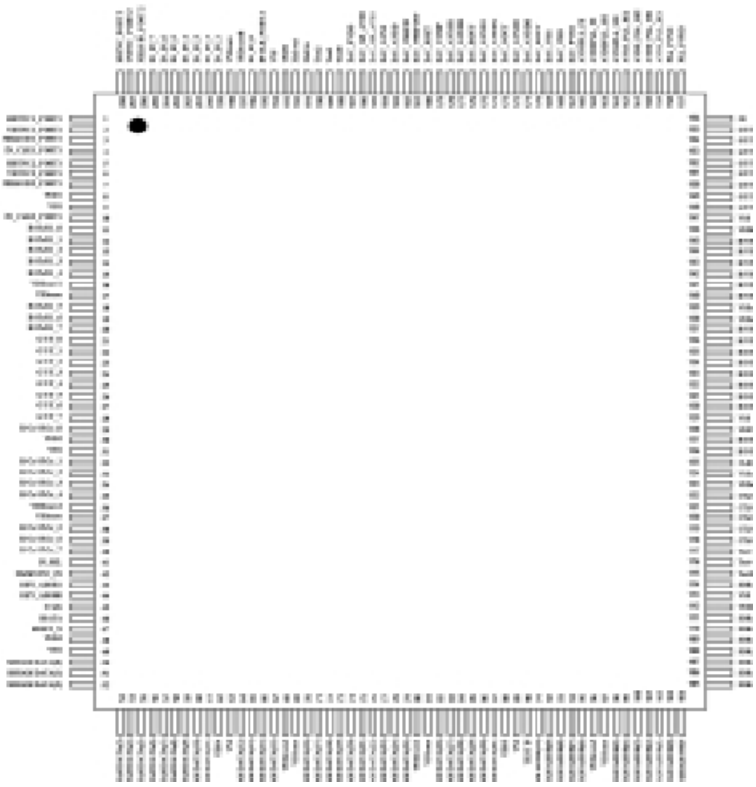


FIGURE 1: Packaging and Pinout Information



Package: 208-pin PQFP ja = TBD °C/watt

SiI161B

General Description

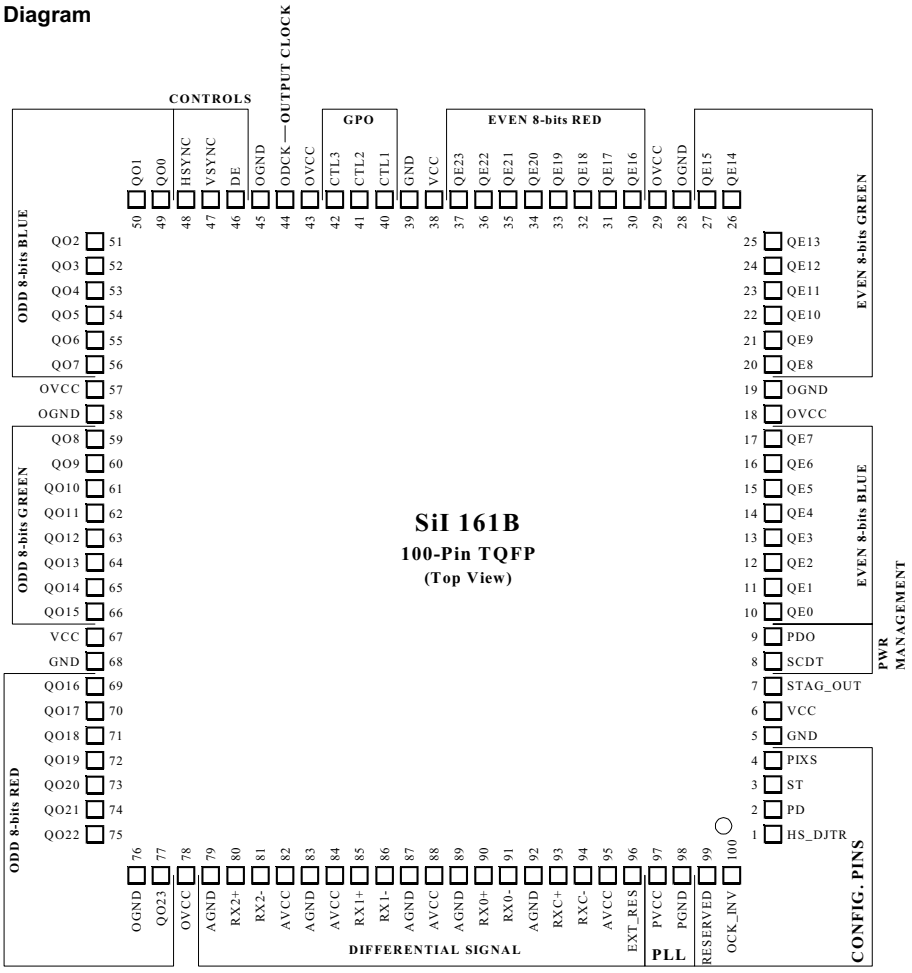
The SiI 161B receiver uses PanelLink Digital technology to support high resolution displays up to UXGA. The SiI 161B receiver supports up to true color panels (24 bit/pixel, 16.7M colors) in 1 or 2 pixels/clock mode. In addition, the receiver data output is time staggered to reduce ground bounce that affects EMI. All PanelLink products are designed on a scaleable CMOS architecture. This ensures support for future performance requirements while maintaining the same logical interface. With this scalable architecture, system designers can be assured that the interface will be fixed through a number of technology and performance generations.

PanelLink Digital technology simplifies PC and display interface design by resolving many of the system level issues associated with high-speed mixed signal design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

Features

- Low Power Operation: 280mA max. current consumption at 3.3V core operation
- Time staggered data output for reduced ground bounce
- Sync Detect: for Plug & Display "Hot Plugging"
- Cable Distance Support: over 5m with twisted-pair, fiber-optics ready
- ESD tolerant to 5kV(HBM on all pins)
- Compliant with DVI 1.0 (DVI is backwards compatible with VESA® P&D™ and DFP)
- Hsync Dejitter Circuitry
- Low power standby mode with clock detect circuitry

SiI161B Pin Diagram



Silicon Image, Inc.

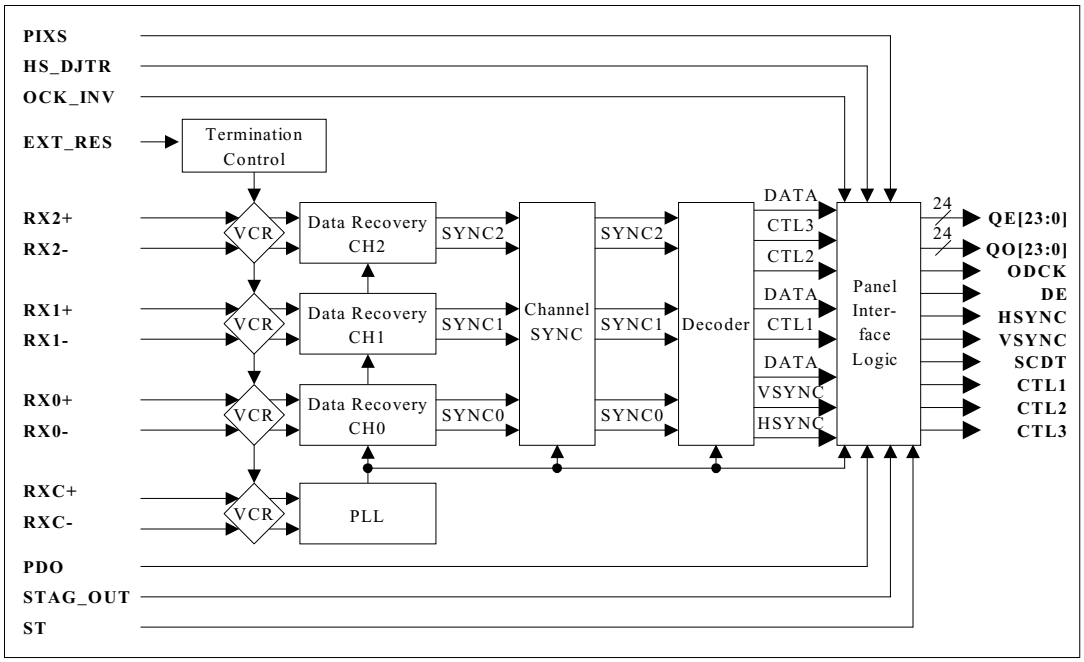
Differences Between Sil161A and Sil161B

While the Sil161B is pin to pin compatible with the Sil161A, there are minor differences in functions and suggested external component value. When designing the Sil161B into an existing design, note that the recommended external resistor (EXT_RES) value has changed from 560 to 390 to match the impedance of a 50 cable. Pin 1 of the Sil161A functions as a selection between Single Link and Dual Link mode. The Sil161B does not support Dual Link operation. Instead pin 1 is used to enable or disable the HSYNC Dejitter function. Table 1 lists the differences between Sil161A and Sil161B.

Pin/Function	Sil161A	Sil161B
Pin 1	S_D: to select Single/Dual Link mode. Pull high to select Dual Link and Pull low for Single Link.	HS_DJTR: to enable HSYNC Dejitter circuitry. Pull high to enable, Pull low to disable.
Pin 4	PIXS/M_S	PIXS
Pin 7	STAG_OUT/SYNCO	STAG_OUT
EXT_RES Resistor Value	560 390	

Table 1. Sil161A vs. Sil161B pin differences.

Functional Block Diagram



TA2024

GENERAL DESCRIPTION

The TA2024 is a 15W/ch continuous average two-channel Class-T Digital Audio Power Amplifier IC using Tripath's proprietary Digital Power Processing™ technology. Class-T amplifiers offer both the audio fidelity of Class-AB and the power efficiency of Class-D amplifiers.

APPLICATIONS

- Computer/PC Multimedia
- DVD Players
- Cable Set-Top Products
- Televisions
- Video CD Players
- Battery Powered Systems

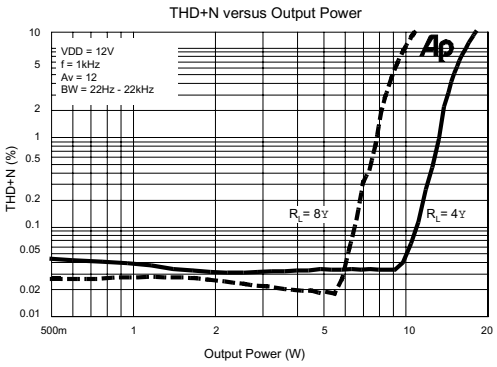
BENEFITS

- Fully integrated solution with FETs
- Easier to design-in than Class-D
- Reduced system cost with no heat sink
- Dramatically improves efficiency versus Class-AB
- Signal fidelity equal to high quality linear amplifiers
- High dynamic range compatible with digital media such as CD, DVD, and Internet audio

FEATURES

- Class-T architecture
- Single Supply Operation
- "Audiophile" Quality Sound
  - 0.04% THD+N @ 9W, 4Ω
  - 0.18% IHF-IM @ 1W, 4Ω
  - 11W @ 4Ω, 0.1% THD+N
  - 6W @ 8Ω, 0.1% THD+N
- High Power
  - 15W @ 4Ω, 10% THD+N
  - 10W @ 8Ω, 10% THD+N
- High Efficiency
  - 81% @ 15W, 4Ω
  - 88% @ 10W, 8Ω
- Dynamic Range = 102 dB
- Mute and Sleep inputs
- Turn-on & turn-off pop suppression
- Over-current protection
- Over-temperature protection
- Bridged outputs
- 36-pin Power SOP package

TYPICAL PERFORMANCE



ABSOLUTE MAXIMUM RATINGS (Note 1)

SYMBOL	PARAMETER	Value	UNITS
V_{DD}	Supply Voltage	16	V
V5	Input Section Supply Voltage	6.0	V
SLEEP	SLEEP Input Voltage	-0.3 to 6.0	V
MUTE	MUTE Input Voltage	-0.3 to V5+0.3	V
T_{STORE}	Storage Temperature Range	-40 to 150	°C
T_A	Operating Free-air Temperature Range	0 to 70	°C
T_J	Junction Temperature	150	°C

Note 1 : Absolute Maximum Ratings indicate limits beyond which damage to the device may
Note 2 : See Power Dissipation Derating in the Applications Information section.

OPERATING CONDITIONS (Note 4)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{DD}	Supply Voltage	8.5	12	13.2	V
V_{IH}	High-level Input Voltage (MUTE, SLEEP)	3.5			V
V_{IL}	Low-level Input Voltage (MUTE, SLEEP)			1	V

Note 3: Recommended Operating Conditions indicate conditions for which the device is fun
See Electrical Characteristics for guaranteed specific performance limits.

ELECTRICAL CHARACTERISTICS

See Test/Application Circuit. Unless otherwise specified, V_{DD} = 12V, f = 1kHz, Measurem
Bandwidth = 22kHz, R_L = 4Y, T_A = 25q C, Package heat slug soldered to 2.8 square-inch F

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
P_O	Output Power (Continuous Average/Channel)	THD+N = 01% R_L = 4 R_L = 8 THD+N = 10% R_L = 4 R_L = 8	9 5.5 12 8	11 6 15 10		W W W W
$I_{DD,MUTE}$	Mute Supply Current	MUTE = V_{IH}		5.5	7	mA
$I_{DD, SLEEP}$	Sleep Supply Current	SLEEP = V_{IH}		0.25	2	mA
I_q	Quiescent Current	V_{IN} = 0 V		61	75	mA
THD + N	Total Harmonic Distortion Plus Noise	P_O = 9W/Channel		0.04		%
IHF-IM	IHF Intermodulation Distortion	19kHz, 20kHz, 1:1 (IHF)		0.18	0.5	%
SNR	Signal-to-Noise Ratio	A-Weighted, P_{OUT} = 1W, R_L = 8	89			dB
CS	Channel Separation	30kHz Bandwidth	50	55		dB
PSRR	Power Supply Rejection Ratio	Vripple = 100mV	60	80		dB
j	Power Efficiency	P_{OUT} = 10W/Channel, R_L = 8		88		%
V_{OFFSET}	Output Offset Voltage	No Load, MUTE = Logic Low		50	150	mV
V_{OH}	High-level output voltage (FAULT & OVER LOAD)	3.5				V
V_{OL}	Low-level output voltage (FAULT & OVER LOAD)				1	V
e_{OUT}	Output Noise Voltage	A-Weighted, input AC grounded		100		oV

Note: Minimum and maximum limits are guaranteed but may not be 100% tested.

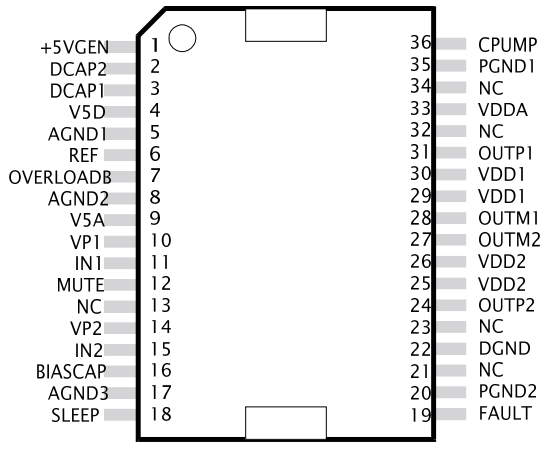
PIN DESCRIPTION

Pin	Function	Description
2, 3	DCAP2, DCAP1	Charge pump sw itching pins. DCAP1 (pin 3) is a free running 300kHz square wave between VDDA and DGND (12Vpp nominal). DCAP2 (pin 2) is level shifted 10 volts above DCAP1 (pin 3) w ith the same amplitude (12Vpp nominal), frequency, and phase as DCAP1.
4, 9	V5D, V5A	Digital 5VDC, Analog 5VDC
5, 8, 17	AGND1, AGND2, AGND3	Analog Ground
6	REF	Internal reference voltage; approximately 1.0 VDC.
7	OVERLOADB	A logic low output indicates the input signal has overloaded the amplifier.
10, 14	VP1, VP2	Input stage output pins.
11, 15	IN1, IN2	Single-ended inputs. Inputs are a “virtual” ground of an inverting opamp w ith approximately 2.4VDC bias.
12	MUTE	When set to logic high, both amplifiers are muted and in idle mode. When low (grounded), both amplifiers are fully operational. If left floating, the device stay s in the mute mode. This pin should be tied to GND if not used.
16	BIASCAP	Input stage bias voltage (approximately 2.4VDC).
18	SLEEP	When set to logic high, device goes into low power mode. If not used, this pin should be grounded
19	FAULT	A logic high output indicates thermal overload, or an output is shorted to ground, or another output.
20, 35	PGND2, PGND1	Pow er Grounds (high current)
22	DGND	Digital Ground
24, 27; 31, 28	OUTP 2 & OUTM2; OUTP 1 & OUTM1	Bridged outputs
25, 26, 29, 30	VDD2, VDD2 VDD1, VDD1	Supply pins for high current H-bridges, nominally 12VDC.
13, 21, 23, 32, 34	NC	Not connected. Not bonded internally .
33	VDDA	Analog 12VDC
36	CPUMP	Charge pump output (nominally 10V above VDDA)
1	5VGEN	Regulated 5VDC source used to supply power to the input section (pins 4 and 9).

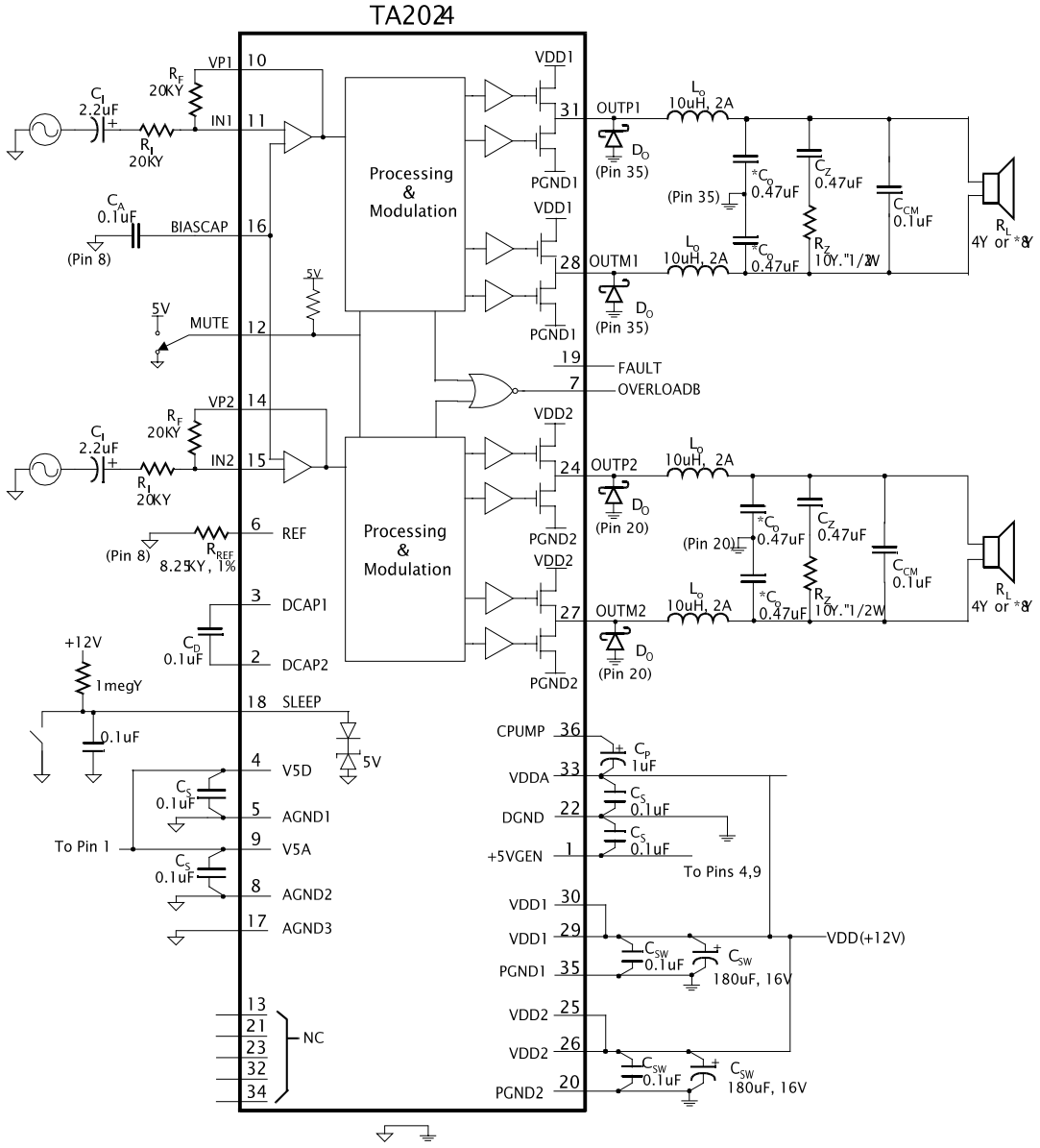
TA2024 PINOUT

36-pin Power SOP Package

(Top View)



APPLICATION /TEST CIRCUIT



Note: Analog and Digital/Power Grounds must be connected locally at the TA2024

Analog Ground

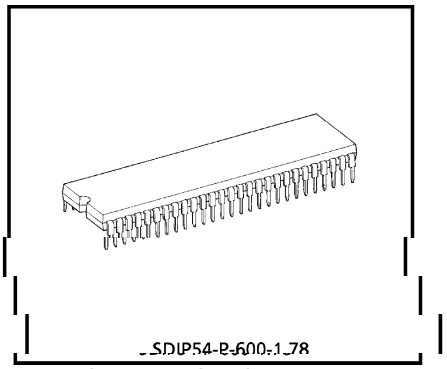
Digital/Power Ground

All Diodes Motorola MBRS130T3

* Use C_O = 0.22uF for 8 Ohm loads

TA8851

The TA8851BN/CN is an A/V SWITCH IC, which has 7 input channels and 2 output channels. Because the 2 output channels can be switched independently of each other, the TA8851BN/CN allows you to configure a PIP system input switching circuit easily.
The TA8851BN/CN can be interfaced easily to a microcontroller via the I^2C bus.
3 of 7 input channels can be used for Y/C separated input.



Weight : 1.0g (Typ.)

FEATURES

Video Stage

- Input
  - Composite video input : 7 channels
  - Y/C input : 3 channels
- Output
  - Composite video output : 2 channels (Main and Sub)
  - Y/C output : 2 channels (Main and Sub)

Audio Stage

- Input
  - L/R input : 7 channels
- Output
  - L/R output : 3 channels (2 of 3 depend on video, and the other is selectable from Main or Sub)

Functions

- I^2C bus interface
- External mute circuit
- DAC output (3 outputs)
- Video clamp circuit
- Mode output
- ADC input (4 inputs)

980910EBA2

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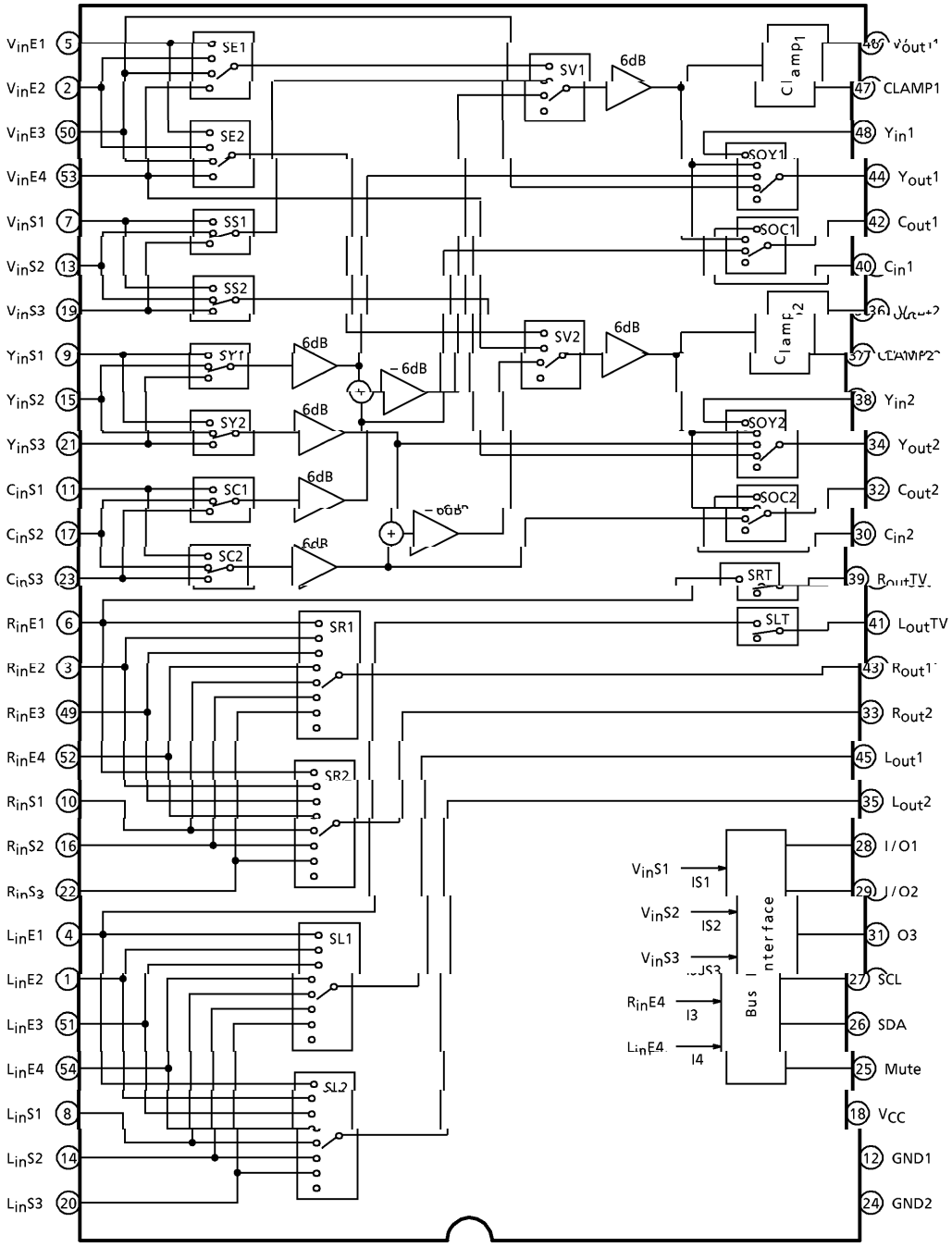
BLOCK DIAGRAM
TA8851BN



VPC3230

1. Introduction

The VPC 323xD is a high-quality, single-chip video front-end, which is targeted for 4:3 and 16:9, 50/60-Hz and 100/120 Hz TV sets. It can be combined with other members of the DIGIT3000 IC family (such as DDP 331x) and/or it can be used with 3rd-party products.

The main features of the VPC 323xD are

- high-performance adaptive 4H comb filter Y/C separator with adjustable vertical peaking
- multi-standard color decoder PAL/NTSC/SECAM including all substandards
- four CVBS, one S-VHS input, one CVBS output
- two RGB/YC_rC_b component inputs, one Fast Blank (FB) input
- integrated high-quality A/D converters and associated clamp and AGC circuits
- multi-standard sync processing
- linear horizontal scaling (0.25 ... 4), as well as non-linear horizontal scaling ("Panoramavision")
- PAL+ preprocessing
- line-locked clock, data and sync, or 656-output interface
- peaking, contrast, brightness, color saturation and tint for RGB/YC_rC_b and CVBS/S-VHS
- high-quality soft mixer controlled by Fast Blank
- PIP processing for four picture sizes ($\frac{1}{4}$, $\frac{1}{9}$, $\frac{1}{16}$, or $\frac{1}{36}$ of normal size) with 8-bit resolution
- 15 predefined PIP display configurations and expert mode (fully programmable)
- control interface for external field memory
- I^2C-bus interface
- one 20.25-MHz crystal, few external components
- 80-pin PQFP package

1.1. System Architecture

Fig.1ñ1 shows the block diagram of the video processor

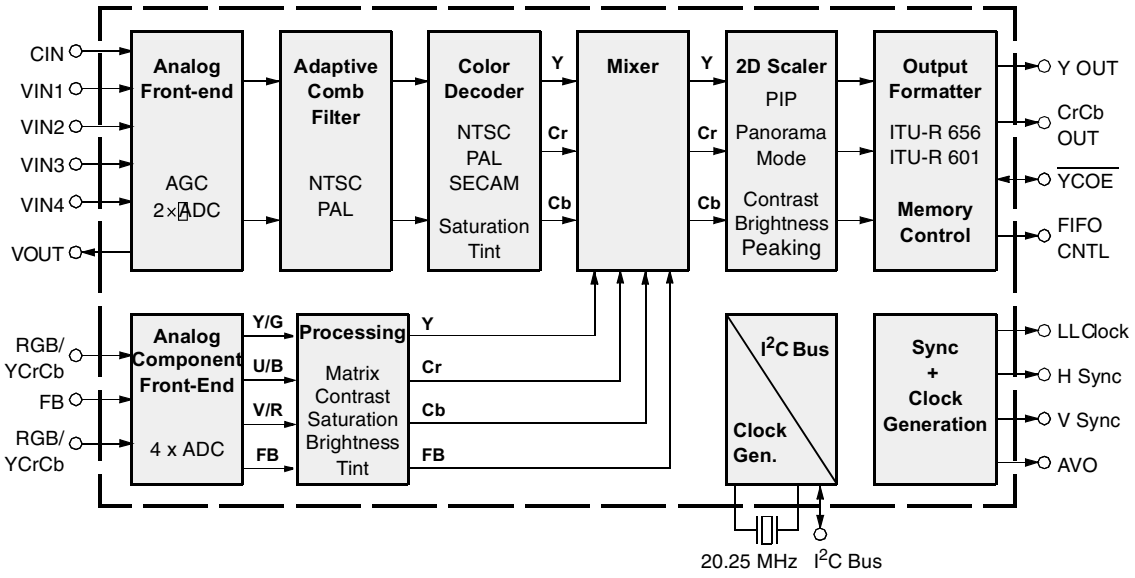


Fig. 1ñ1: Block diagram of the VPC 323xD

1.2. Video Processo rFamily

The VPC video pro cessor family supports 15/32-kHz systems and is available with different comb filter options. Table 1ñ1 gives an overview of the VPC video proc es sor family.

Table 1ñ1: VPC Processor Family for 100 Hz, Double-Scan and Line-Locked Clock Applications

	Features				
Type	Adaptive Comb filter (PAL/NTSC)	Panorama Vision	Analog Component Inputs	Vertical Scaler (PIP)	Digital Output Interface
VPC 3230D	4H	3	2	3	ITU-R 601, ITU-R 656
VPC 3231D		3	2	3	ITU-R 601, ITU-R 656
VPC 3232D	4H	3	3		ITU-R 601, ITU-R 656
VPC 3233D		3	3		ITU-R 601, ITU-R 656
VPC 3215C	4H	3			ITU-R 601
VPC 3210A	2H	3			ITU-R 601
VPC 3211A		3			ITU-R 601

1.3. VPC Applications

Fig. 1ñ2 depicts several VPC applications. Since the VPC functions as a video front-end, it must be complemented with additional functionality to form a complete TV set.

The DDP 331x contains the video back-end with video postprocessing (contrast, peaking, CTI,...), H/V-deflection, RGB insertion (SCART, Text, PIP,...) and tube control (cutoff, white-drive, beam current limiter). It generates a beam scan velocity modulation output from the digital YC_rC_b and RGB signals. Note, that this signal is not generated from the external analog RGB inputs.

The component interface of the VPC 323xD provides a high-quality analog RGB interface with character insertion capability. It also allows appropriate processing of external sources, such as MPEG-2 set-top boxes in transparent (4:2:2) quality. Furthermore, it transforms RGB/Fast Blank signals to the common digital video bus and makes those signals available for 100-Hz upconversion or double-scan processing. In some European countries (Italy), this feature is mandatory.

SRC (e. g. SDA 94xx from Micronas) indicates memory based image processing, such as scan rate conversion, vertical processing (Zoom), or PAL+ reconstruction. The VPC supports memory-based applications through line-locked clocks, syncs, and data. Additionally, the VPC 323xD provides a 656-output interface and FIFO control signals.

Examples:

- Europe: 15 kHz/50 Hz Æ 32 kHz/100 Hz interlaced
- US: 15 kHz/60 Hz Æ 32 kHz/60 Hz non-interlaced

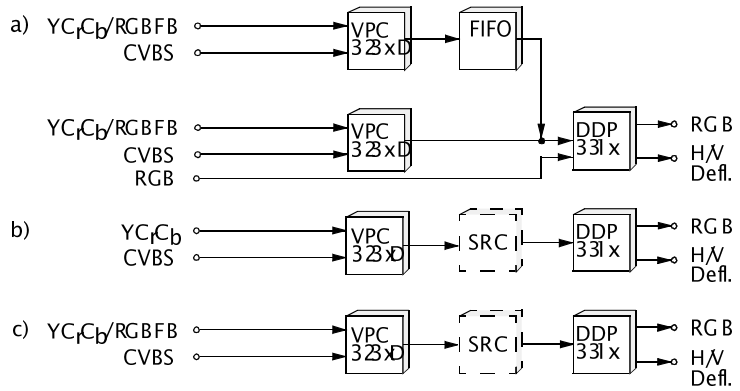


Fig. 1ñ2: VPC 32xxD applications
a) 15-kHz application Europe
b) double-scan application (US, Japan) with YC_rC_b inputs
c) 100-Hz application (Europe) with RGB FB inputs

uPD64083

PD64083 realizes a high precision Y/C separation and a noise reduction by the three-dimension signal processing for NTSC signal.
This product has the On-chip 4Mbit memory for flame delay, 2ch of high precision internal 10bit A/D converter, and adapting 10bit signal processing (only for luminance signal) and high picture quality. PD64083 is completely single chip system of 3DY/C separation.
This LSI includes the Wide Clear Vision ID signal (Japanese local format) decoder and ID-1 signal decoder.

FEATURES

- On-chip 4Mbit frame delay memory.
- 3 Operation mode (Compatible to PD64082)
  - Motion adaptive 3D Y/C separation
  - Frame recursive Y/C NR (for Y/C separated video input)
  - 2D Y/C separation + Frame recursive Y/C NR (for Composite video input)
- Embedded a high performance pipeline 10bit A/D converter (2ch)
- Embedded system clock generator, 2ch of D/A converter, Y coring, Vertical enhancer, Peaking filter, and Noise detector.
- Include ID-1 signal decoder
- I2C bus control.
- Dual power supply of 2.5V and 3.3V.
  - For digital : DVDD = 2.5V
  - For analog : AVDD = 2.5V
  - For DRAM : DVDDRAM = 2.5V
  - For I/O : DVDDIO = 3.3V

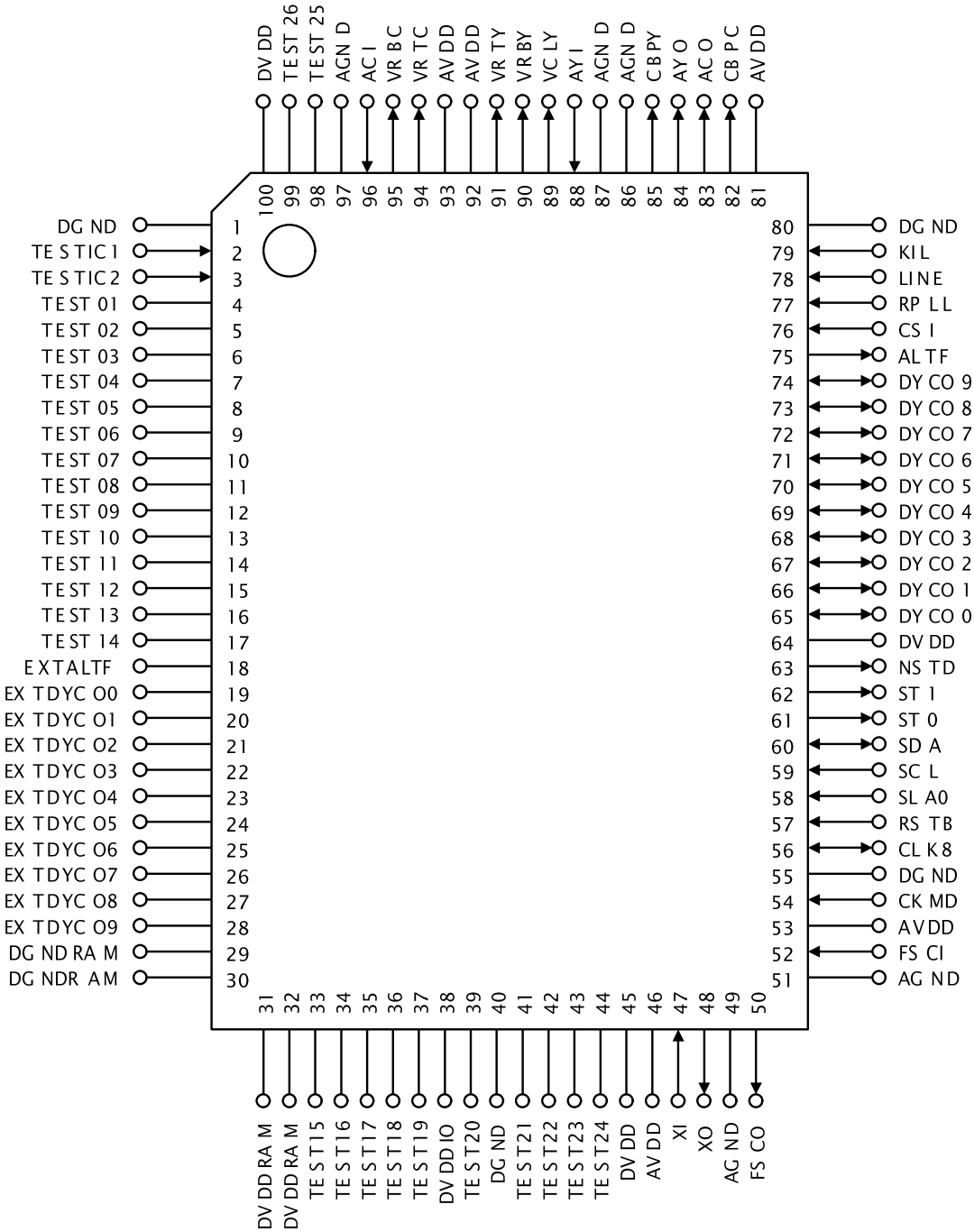
ORDERING INFORMATION

Part number	Package
PD64083GF-3BA	100-pin plastic QFP (14 20)

PIN CONFIGURATION (TOP VIEW)

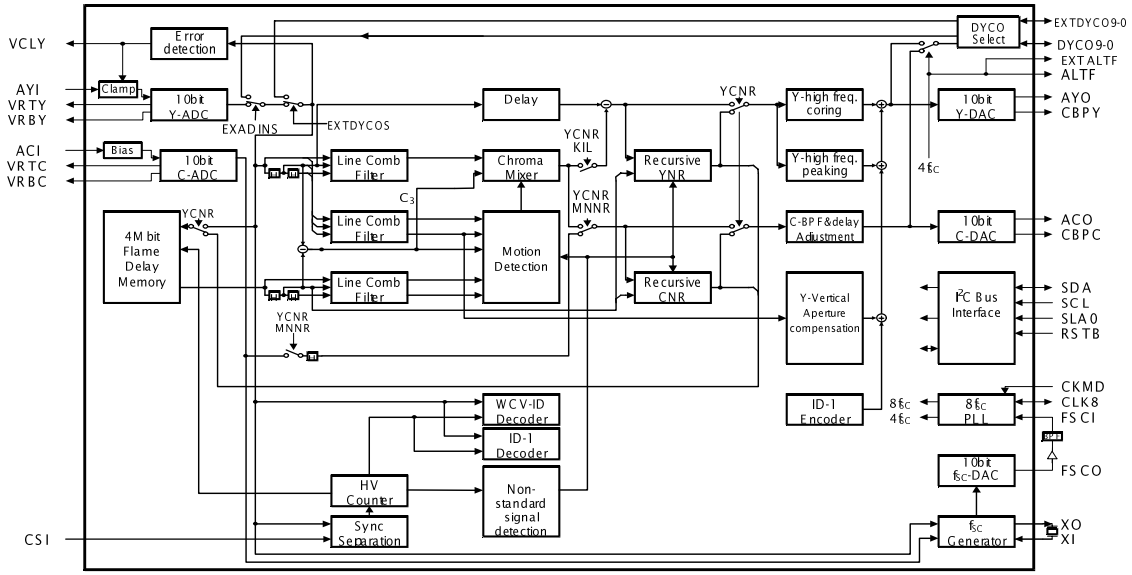
100-pin plastic QFP (14 20)

PD 64083GF-3BA



ACI : Analog C (Chroma) Signal Input
ACO : Analog C (Chroma) Signal Output
AGND : Analog Section Ground
ALTF : Alternate Flag for Digital Y/C Output
AVDD : Analog Section Power Supply
AYI : Analog Y (Luma) Signal Input
AYO : Analog Y (Luma) Signal Output
CBPC : C-DAC Phase Compensation Output
CBPY : Y-DAC Phase Compensation Output
CKMD : Clock Mode Selection
CLK8 : 8-SC Clock Input / Output
CSI : Composite Sync. Input
DGND : Digital Section Ground
DVDD : Digital Section Power Supply
DYCO0 - DYCO9 : Digital Y/C Signal (Alternative) Outputs
EXTALTF : Extend Alternate Flag for Digital Y/C Output
EXTDYCO0 – EXTDYCO9 : Extend Digital Y/C Signal (Alternative) Outputs
FSCI : -SC (Subcarrier) Input
FSCO : -SC (Subcarrier) Output
KIL : Killer Selection
LINE : Inter-Line Separate Selection
NSTD : Non Standard Detection Monitor
RPLL : Testing Selection
RSTB : System Reset (Negative)
SCL : Serial Clock Input
SDA : Serial Data Input / Output
SLA0 : Slave Address Selection
ST1, ST0 : Inner States Monitor
TEST 01 – TEST 26 : Testing Selection
TEST IC1 - TEST IC2 : IC Testing Section
VCLY : Clamp Voltage Output for Y-ADC
VRTC : Top Voltage Reference Output for C-ADC
VRTY : Top Voltage Reference Output for Y-ADC
VRBC : Bottom Voltage Reference Output for C-ADC
VRBY : Bottom Voltage Reference Output for Y-ADC
XI : X'TAL input
XO : X'TAL output

BLOCK DIA GRAM



Hyundai ImageQuest

PT421H

Working Board Schematic(GRAPHIC)

(ASI500)

01. Cover Page
02. Block Diagram
03. VGA Analog Input
04. CXA2151Q
05. ADC-AD9883(140M)
06. TMDS RECEIVER SIL161B-140
07. Damping Network
08. ASI500
09. ASI500 DECOUPLE CAPS
10. FRAME BUFFER MEMORY
11. LVDS TRANSMITTER(DS90C385MTD)
12. MSP3450G AUDIO PROCESSOR
13. MicroController SDA5550
14. Power Distribution
15. MAX232

Date:05/29/2003

Hyundai ImageQuest		
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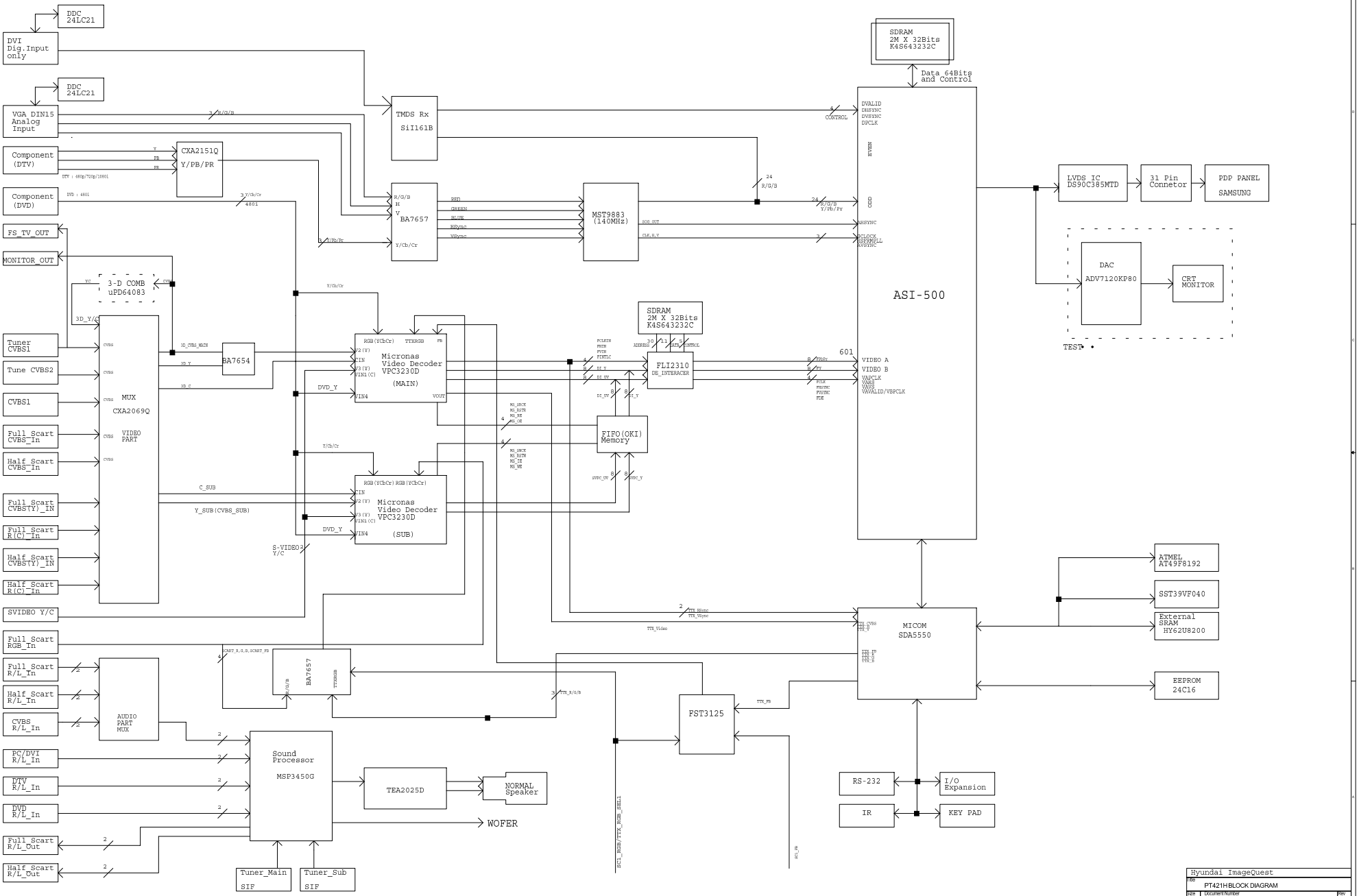
Size: B	Document Number: E42095419	Rev: 1.0
Date: Thursday, September 18, 2003	Sheet 1 of 15	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DVI Dig.Input only
DDC 24LC21
VGA DIN15 Analog Input
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Component (DVD)
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MONITOR_OUT
CXA2151Q Y/PB/PR
TMDS Rx SiI161B
R/G/B H V BA7657
Y/Cb/Cr
MST9883 (140MHz)
SDRAM 2M X 32Bits K4S643232C
Data 64Bits and Control
ASI-500
LVDS IC DS90C385MTD
31 Pin Connetor
PDP PANEL SAMSUNG
DAC ADV7120KP80
CRT MONITOR
TEST
3-D COMB uPD64083
MUX CXA2069Q
VIDEO PART
Tuner CVBS1
Tune CVBS2
CVBS1
Full_Scart CVBS_In
Half_Scart CVBS_In
Full_Scart CVBS(Y)_IN
Full_Scart R(C)_In
Half_Scart CVBS(Y)_IN
Half_Scart R(C)_In
SVIDEO Y/C
Full_Scart RGB_In
BA7654
Micronas Video Decoder VPC3230D (MAIN)
Micronas Video Decoder VPC3230D (SUB)
SDRAM 2M X 32Bits K4S643232C
FLI2310 DE_INTERACER
FIFO(OKI) Memory
S-VIDEO Y/C
C_SUB
Y_SUB(CVBS_SUB)
BA7657
MICOM SDA5550
ATMEL AT49F8192
SST39VF040
External SRAM HY62U8200
EEPROM 24C16
Full_Scart R/L_In
Half_Scart R/L_In
CVBS R/L_In
AUDIO PART MUX
PC/DVI R/L_In
DTV R/L_In
DVD R/L_In
Full_Scart R/L_Out
Half_Scart R/L_Out
Sound Processor MSP3450G
TEA2025D
NORMAL Speaker
WOFER
Tuner_Main SIF
Tuner_Sub SIF
FST3125
RS-232
IR
I/O Expansion
KEY PAD
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Rev 1.0
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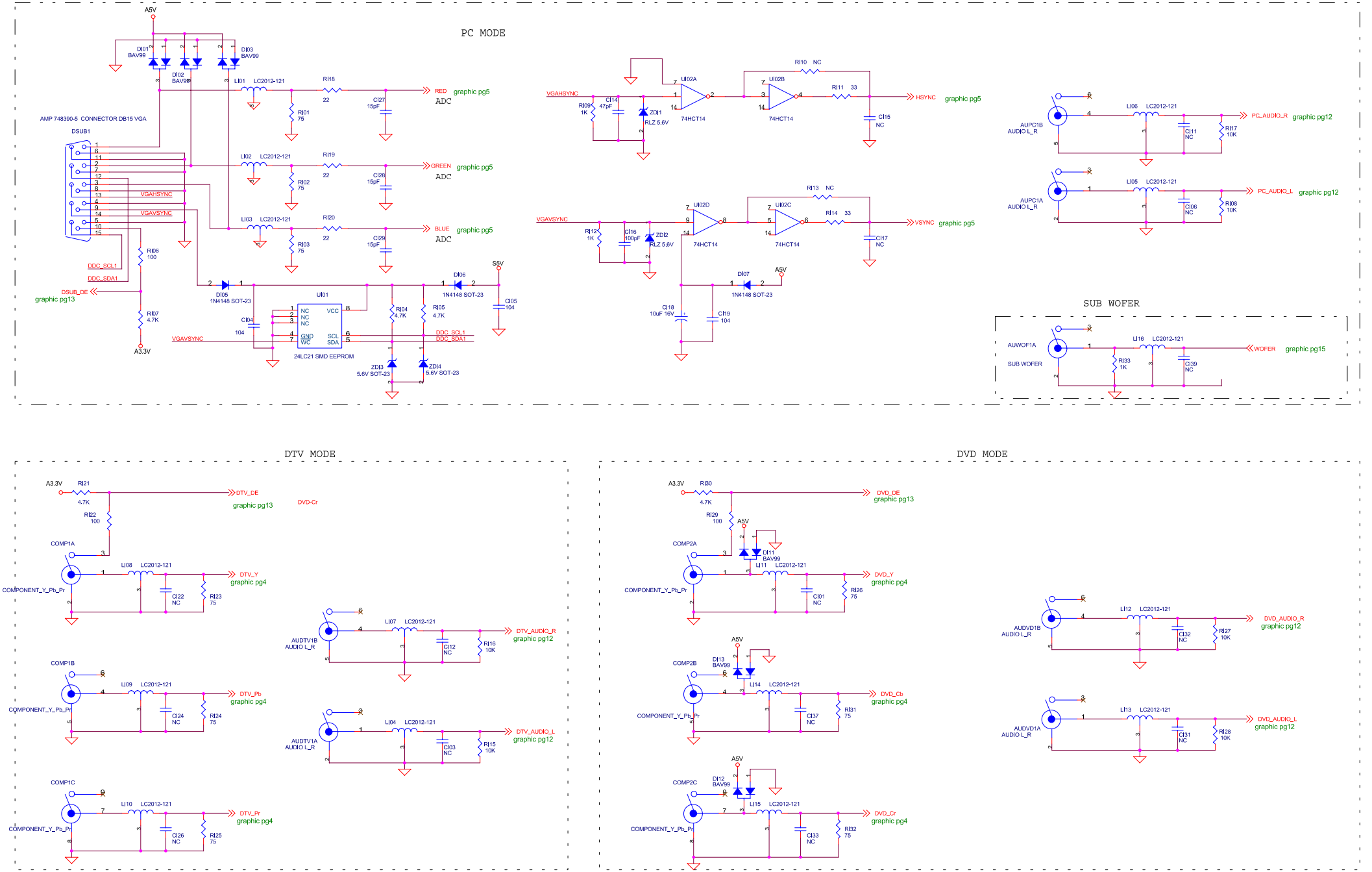
Sheet 2 of 15


PC MODE
A5V
DI01 BAV99
DI02 BAV99
DI03 BAV99
AMP 748390-5 CONNECTOR DB15 VGA
DSUB1
LI01 LC2012-121
LI02 LC2012-121
LI03 LC2012-121
RI18 22
RI19 22
RI20 22
RI01 75
RI02 75
RI03 75
CI27 15pF
CI28 15pF
CI29 15pF
RED graphic pg5
ADC
GREEN graphic pg5
ADC
BLUE graphic pg5
ADC
VGAHSYNC
VGAVSYNC
DDC_SCL1
DDC_SDA1
DSUB_DE graphic pg13
RI06 100
RI07 4.7K
A3.3V
DI05 1N4148 SOT-23
DI06 1N4148 SOT-23
S5V
CI05 104
UI01
24LC21 SMD EEPROM
CI04 104
RI04 4.7K
RI05 4.7K
ZDI3 5.6V SOT-23
ZDI4 5.6V SOT-23
VGAHSYNC
RI09 1K
CI14 47pF
ZDI1 RLZ 5.6V
UI02A 74HCT14
RI10 NC
UI02B 74HCT14
RI11 33
CI15 NC
HSYNC graphic pg5
VGAVSYNC
RI12 1K
CI16 100pF
ZDI2 RLZ 5.6V
UI02D 74HCT14
RI13 NC
UI02C 74HCT14
RI14 33
CI17 NC
VSYNC graphic pg5
DI07 1N4148 SOT-23
CI18 10uF 16V
CI19 104
AUPC1B AUDIO L_R
LI06 LC2012-121
CI11 NC
RI17 10K
PC_AUDIO_R graphic pg12
AUPC1A AUDIO L_R
LI05 LC2012-121
CI06 NC
RI08 10K
PC_AUDIO_L graphic pg12
SUB WOFER
AUWOF1A
SUB WOFER
LI16 LC2012-121
RI33 1K
CI39 NC
WOFER graphic pg15
DTV MODE
A3.3V
RI21 4.7K
RI22 100
DTV_DE graphic pg13
DVD-Cr
COMP1A
LI08 LC2012-121
CI22 NC
RI23 75
DTV_Y graphic pg4
COMPONENT_Y_Pb_Pr
COMP1B
LI09 LC2012-121
CI24 NC
RI24 75
DTV_Pb graphic pg4
COMP1C
LI10 LC2012-121
CI26 NC
RI25 75
DTV_Pr graphic pg4
AUDTV1B AUDIO L_R
LI07 LC2012-121
CI12 NC
RI16 10K
DTV_AUDIO_R graphic pg12
AUDTV1A AUDIO L_R
LI04 LC2012-121
CI03 NC
RI15 10K
DTV_AUDIO_L graphic pg12
DVD MODE
A3.3V
RI30 4.7K
RI29 100
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A5V
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COMP2A
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CI01 NC
RI26 75
DVD_Y graphic pg4
COMPONENT_Y_Pb_Pr
DI13 BAV99
COMP2B
LI14 LC2012-121
CI37 NC
RI31 75
DVD_Cb graphic pg4
DI12 BAV99
COMP2C
LI15 LC2012-121
CI33 NC
RI32 75
DVD_Cr graphic pg4
AUDVD1B AUDIO L_R
LI12 LC2012-121
CI32 NC
RI27 10K
DVD_AUDIO_R graphic pg12
AUDVD1A AUDIO L_R
LI13 LC2012-121
CI31 NC
RI28 10K
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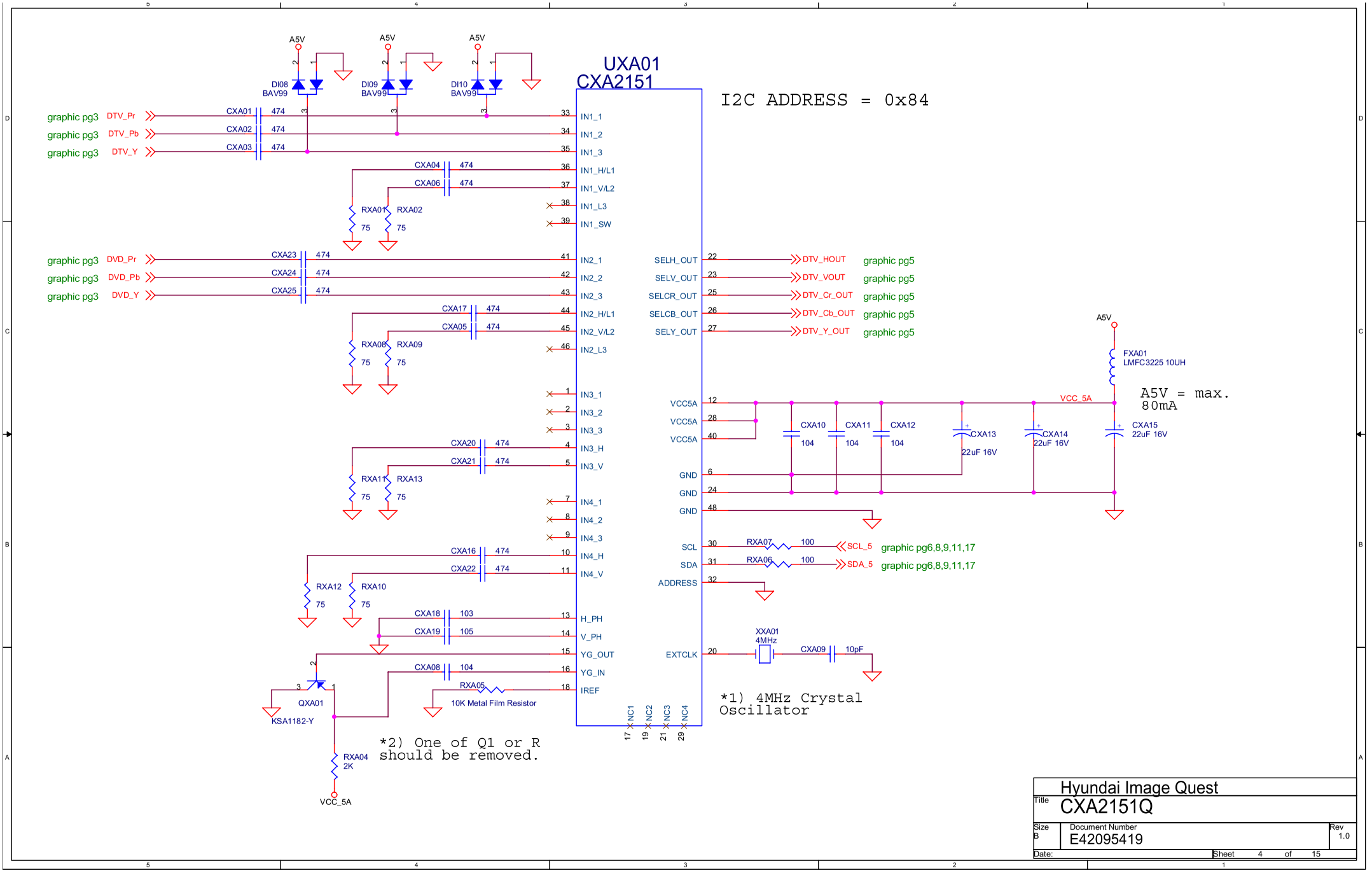
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CXA2151
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A5V
DI08 BAV99
DI09 BAV99
DI10 BAV99
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graphic pg3 DTV_Pb
graphic pg3 DTV_Y
graphic pg3 DVD_Pr
graphic pg3 DVD_Pb
graphic pg3 DVD_Y
CXA01 474
CXA02 474
CXA03 474
CXA04 474
CXA06 474
CXA23 474
CXA24 474
CXA25 474
CXA17 474
CXA05 474
CXA20 474
CXA21 474
CXA16 474
CXA22 474
CXA18 103
CXA19 105
CXA08 104
RXA01 75
RXA02 75
RXA08 75
RXA09 75
RXA11 75
RXA13 75
RXA12 75
RXA10 75
RXA05 10K Metal Film Resistor
RXA04 2K
QXA01
KSA1182-Y
VCC_5A
IN1_1
IN1_2
IN1_3
IN1_H/L1
IN1_V/L2
IN1_L3
IN1_SW
IN2_1
IN2_2
IN2_3
IN2_H/L1
IN2_V/L2
IN2_L3
IN3_1
IN3_2
IN3_3
IN3_H
IN3_V
IN4_1
IN4_2
IN4_3
IN4_H
IN4_V
H_PH
V_PH
YG_OUT
YG_IN
IREF
NC1
NC2
NC3
NC4
SELH_OUT
SELV_OUT
SELCR_OUT
SELCB_OUT
SELY_OUT
DTV_HOUT graphic pg5
DTV_VOUT graphic pg5
DTV_Cr_OUT graphic pg5
DTV_Cb_OUT graphic pg5
DTV_Y_OUT graphic pg5
VCC5A
GND
SCL
SDA
ADDRESS
EXTCLK
RXA07 100
RXA06 100
SCL_5 graphic pg6,8,9,11,17
SDA_5 graphic pg6,8,9,11,17
XXA01 4MHz
CXA09 10pF
*1) 4MHz Crystal Oscillator
*2) One of Q1 or R should be removed.
FXA01 LMFC3225 10UH
A5V = max. 80mA
VCC_5A
CXA10 104
CXA11 104
CXA12 104
CXA13 22uF 16V
CXA14 22uF 16V
CXA15 22uF 16V
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Title CXA2151Q
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Rev 1.0
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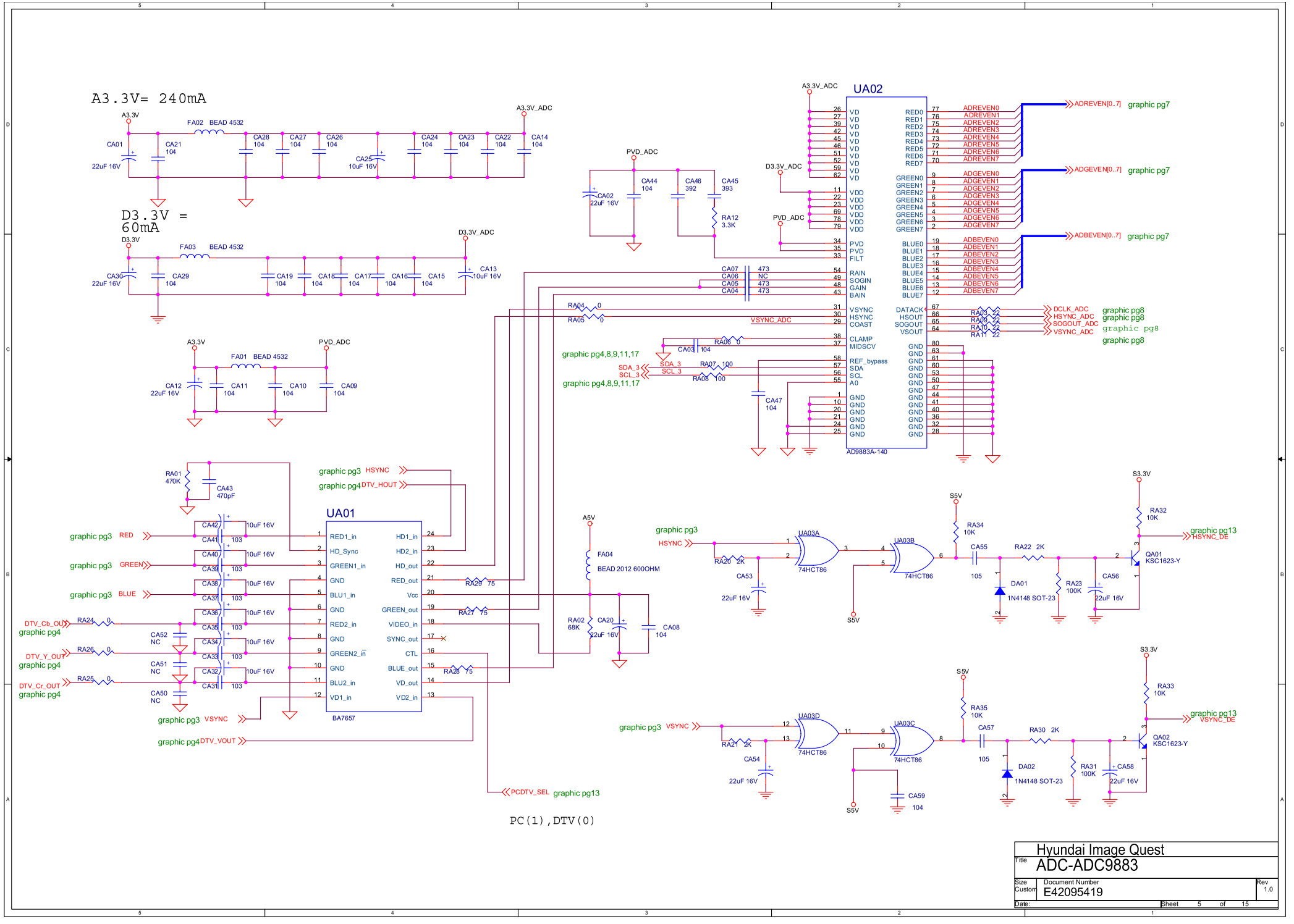
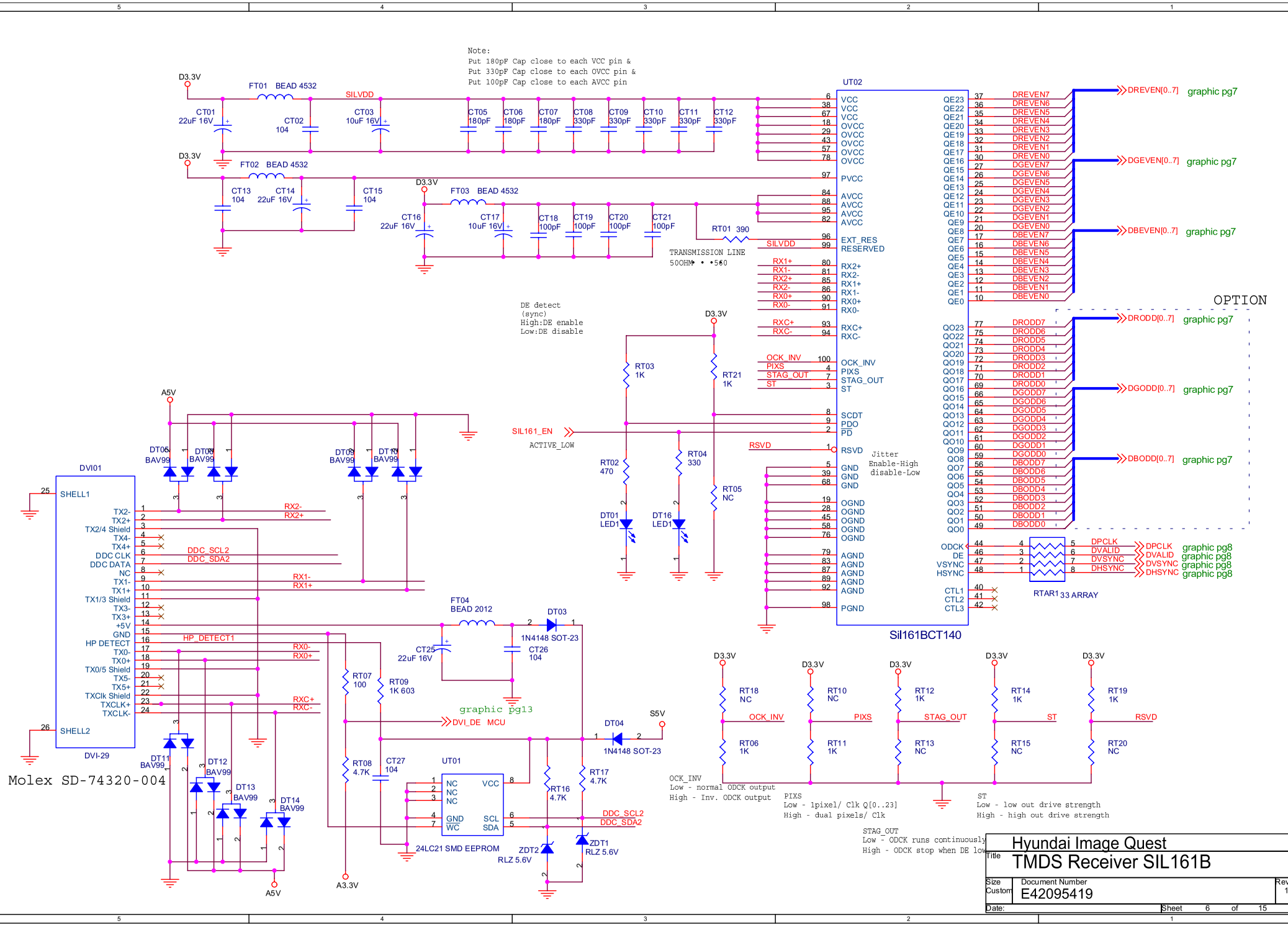
Sheet 4 of 15


A3.3V= 240mA
D3.3V = 60mA
UA02
AD9883A-140
UA01
BA7657
PC(1),DTV(0)
Hyundai Image Quest
ADC-ADC9883
E42095419


Note:
Put 180pF Cap close to each VCC pin &
Put 330pF Cap close to each OVCC pin &
Put 100pF Cap close to each AVCC pin
UT02
Sil161BCT140
DVI01
DVI-29
Molex SD-74320-004
UT01
24LC21 SMD EEPROM
RTAR1 33 ARRAY
TRANSMISSION LINE
50OHM
DE detect
(sync)
High:DE enable
Low:DE disable
SIL161_EN
ACTIVE_LOW
Jitter
Enable-High
disable-Low
OPTION
DREVEN[0..7] graphic pg7
DGEVEN[0..7] graphic pg7
DBEVEN[0..7] graphic pg7
DRODD[0..7] graphic pg7
DGODD[0..7] graphic pg7
DBODD[0..7] graphic pg7
graphic pg8
graphic pg13
DVI_DE MCU
OCK_INV
Low - normal ODCK output
High - Inv. ODCK output
PIXS
Low - 1pixel/ Clk Q[0..23]
High - dual pixels/ Clk
ST
Low - low out drive strength
High - high out drive strength
STAG_OUT
Low - ODCK runs continuously
High - ODCK stop when DE low
Hyundai Image Quest
TMDS Receiver SIL161B
E42095419
Rev 1.0
Sheet 6 of 15

Analog Interface Damping Network

graphic pg5 ADREVEN[0..7] >> ADREVEN[0..7]

RDAR01_33 ARRAY

ADREVEN0	1	8	IREVEN0
ADREVEN1	2	7	IREVEN1
ADREVEN2	3	6	IREVEN2
ADREVEN3	4	5	IREVEN3

RDAR02 33 ARRAY

ADREVEN4	1	8	IREVEN4
ADREVEN5	2	7	IREVEN5
ADREVEN6	3	6	IREVEN6
ADREVEN7	4	5	IREVEN7

IREVEN[0..7] >> IREVEN[0..7] graphic pg8

graphic pg5 ADGEVEN[0..7] >> ADGEVEN[0..7]

RDAR03 33 ARRAY

ADGEVEN0	1	8	IGEVEN0
ADGEVEN1	2	7	IGEVEN1
ADGEVEN2	3	6	IGEVEN2
ADGEVEN3	4	5	IGEVEN3

RDAR04 33 ARRAY

ADGEVEN4	1	8	IGEVEN4
ADGEVEN5	2	7	IGEVEN5
ADGEVEN6	3	6	IGEVEN6
ADGEVEN7	4	5	IGEVEN7

IGEVEN[0..7] >> IGEVEN[0..7] graphic pg8

graphic pg5 ADBEVEN[0..7] >> ADBEVEN[0..7]

RDAR05_33 ARRAY

ADBEVEN0	1	8	IBEVEN0
ADBEVEN1	2	7	IBEVEN1
ADBEVEN2	3	6	IBEVEN2
ADBEVEN3	4	5	IBEVEN3

RDAR06_33 ARRAY

ADBEVEN4	1	8	IBEVEN4
ADBEVEN5	2	7	IBEVEN5
ADBEVEN6	3	6	IBEVEN6
ADBEVEN7	4	5	IBEVEN7

IBEVEN[0..7] >> IBEVEN[0..7] graphic pg8

Digital Interface Damping Network

graphic pg6 DREVEN[0..7] >> DREVEN[0..7]

RDAR13_33 ARRAY

DREVEN0	8	1	IREVEN0
DREVEN1	7	2	IREVEN1
DREVEN2	6	3	IREVEN2
DREVEN3	5	4	IREVEN3

RDAR14_33 ARRAY

DREVEN4	8	1	IREVEN4
DREVEN5	7	2	IREVEN5
DREVEN6	6	3	IREVEN6
DREVEN7	5	4	IREVEN7

IREVEN[0..7] >> IREVEN[0..7] graphic pg8

graphic pg6 DGEVEN[0..7] >> DGEVEN[0..7]

RDAR15_33 ARRAY

DGEVEN0	8	1	IGEVEN0
DGEVEN1	7	2	IGEVEN1
DGEVEN2	6	3	IGEVEN2
DGEVEN3	5	4	IGEVEN3

RDAR16_33 ARRAY

DGEVEN4	8	1	IGEVEN4
DGEVEN5	7	2	IGEVEN5
DGEVEN6	6	3	IGEVEN6
DGEVEN7	5	4	IGEVEN7

IGEVEN[0..7] >> IGEVEN[0..7] graphic pg8

graphic pg6 DBEVEN[0..7] >> DBEVEN[0..7]

RDAR17_33 ARRAY

DBEVEN0	8	1	IBEVEN0
DBEVEN1	7	2	IBEVEN1
DBEVEN2	6	3	IBEVEN2
DBEVEN3	5	4	IBEVEN3

RDAR18_33 ARRAY

DBEVEN4	8	1	IBEVEN4
DBEVEN5	7	2	IBEVEN5
DBEVEN6	6	3	IBEVEN6
DBEVEN7	5	4	IBEVEN7

IBEVEN[0..7] >> IBEVEN[0..7] graphic pg8

OPTION

graphic pg6 DRODD[0..7] >> DRODD[0..7]

RDAR19_33 ARRAY

DRODD0	8	1	IRODD0
DRODD1	7	2	IRODD1
DRODD2	6	3	IRODD2
DRODD3	5	4	IRODD3

RDAR20_33 ARRAY

DRODD4	8	1	IRODD4
DRODD5	7	2	IRODD5
DRODD6	6	3	IRODD6
DRODD7	5	4	IRODD7

IRODD[0..7] >> IRODD[0..7] graphic pg8

graphic pg6 DGODD[0..7] >> DGODD[0..7]

RDAR21_33 ARRAY

DGODD0	8	1	IGODD0
DGODD1	7	2	IGODD1
DGODD2	6	3	IGODD2
DGODD3	5	4	IGODD3

RDAR22_33 ARRAY

DGODD4	8	1	IGODD4
DGODD5	7	2	IGODD5
DGODD6	6	3	IGODD6
DGODD7	5	4	IGODD7

IGODD[0..7] >> IGODD[0..7] graphic pg8

graphic pg6 DBODD[0..7] >> DBODD[0..7]

RDAR23_33 ARRAY

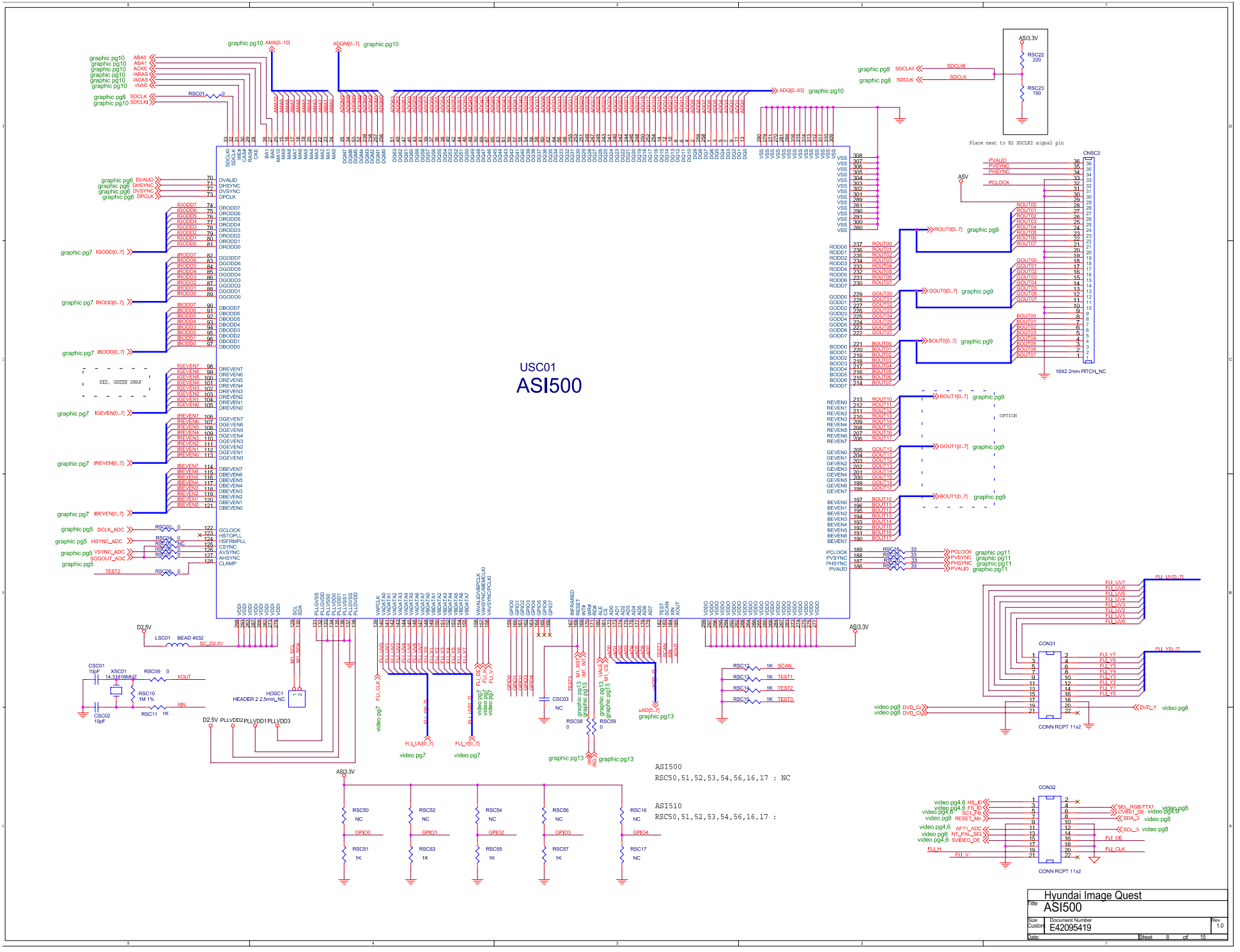
DBODD0	8	1	IBODD0
DBODD1	7	2	IBODD1
DBODD2	6	3	IBODD2
DBODD3	5	4	IBODD3

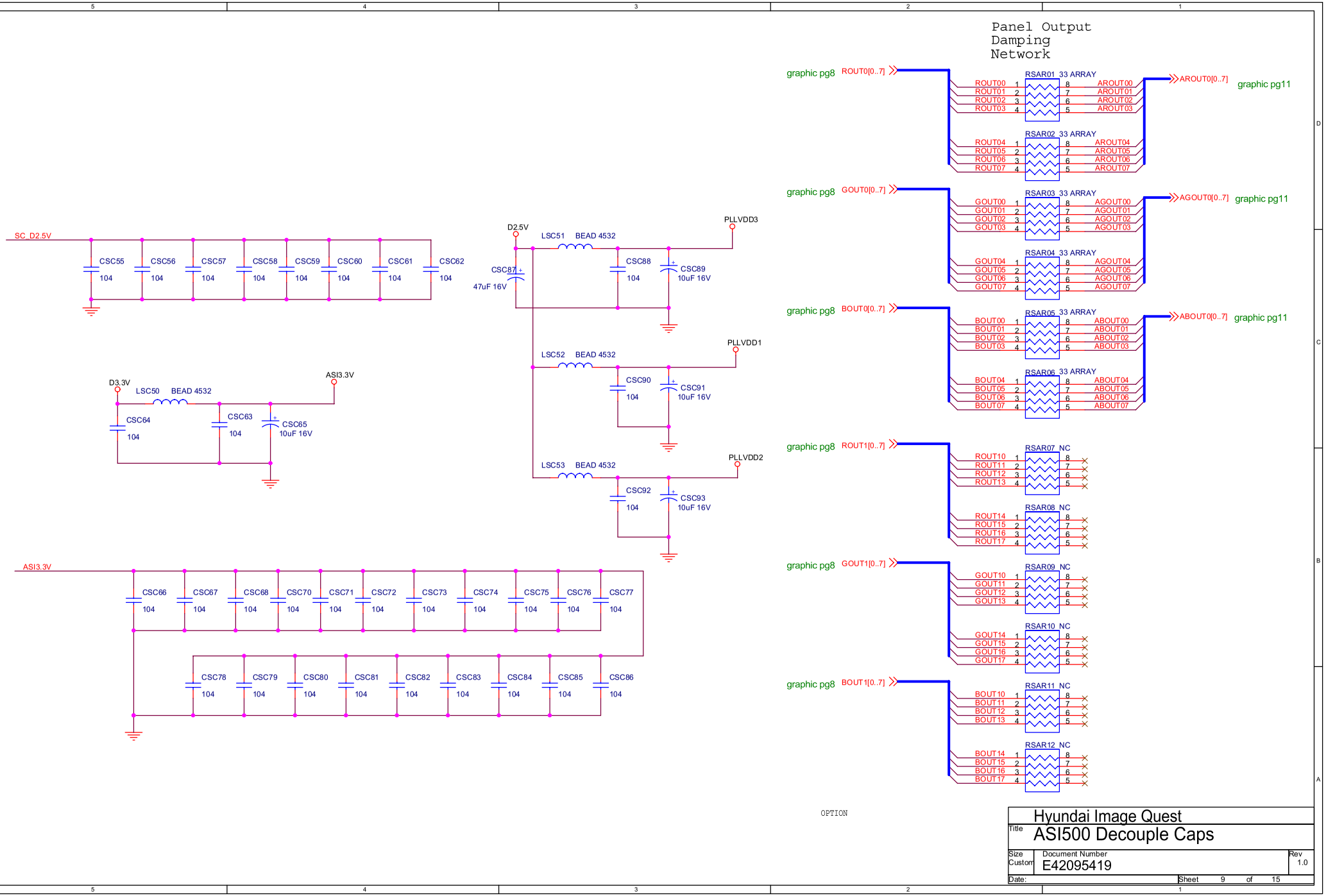
RDAR24_33 ARRAY

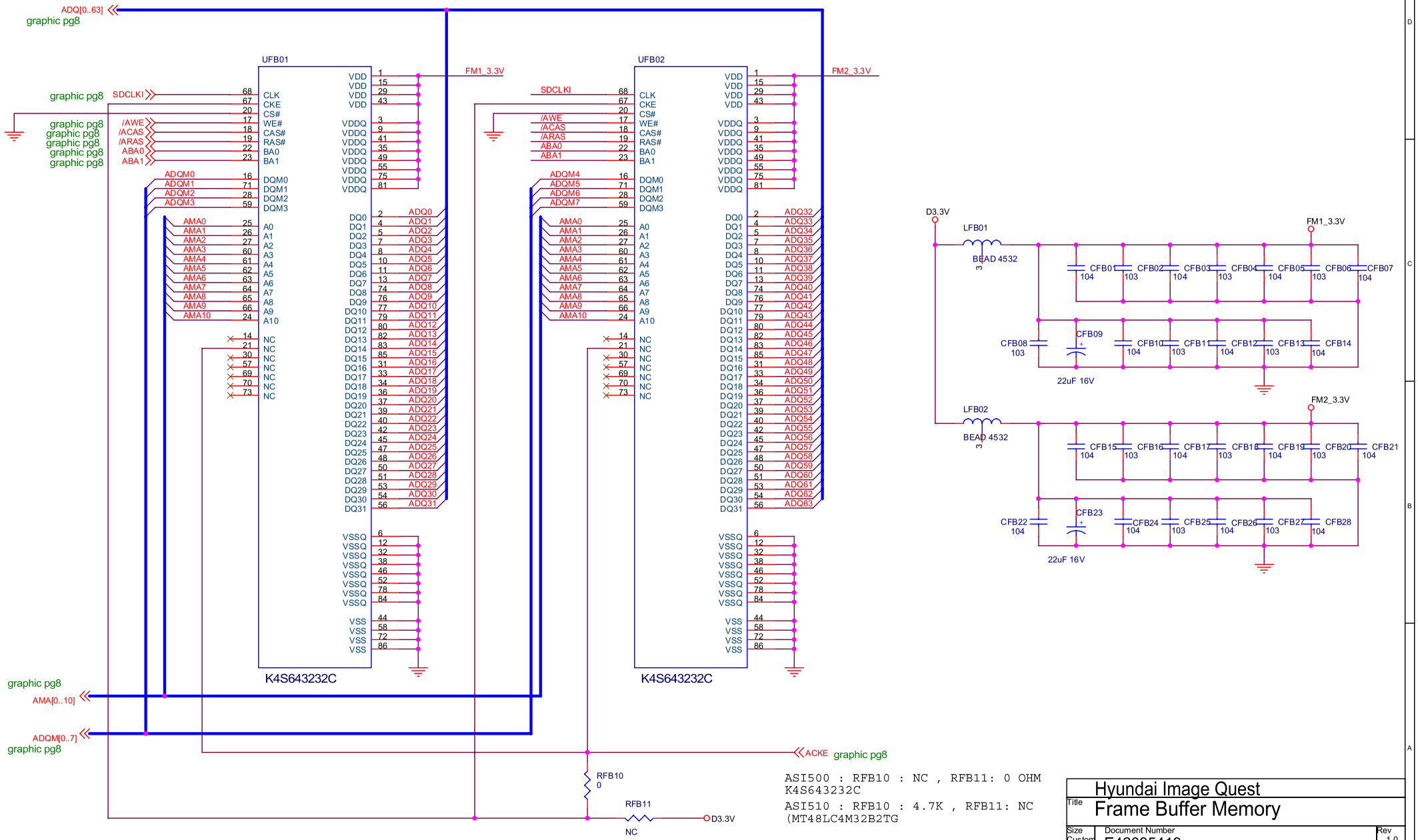
DBODD4	8	1	IBODD4
DBODD5	7	2	IBODD5
DBODD6	6	3	IBODD6
DBODD7	5	4	IBODD7

IBODD[0..7] >> IBODD[0..7] graphic pg8

	Hyundai Image Quest
Title	Damping Network
Size C	Document Number E42095419
Rev	1.0
Date:	Sheet 7 of 15


USC01
ASI500
ASI3.3V
D2.5V
RED, GREEN SWAP
Place next to H2 SDCLKI signal pin
16X2 2mm PITCH_NC
CONN RCPT 11x2
CONN RCPT 11x2
ASI500
RSC50,51,52,53,54,56,16,17 : NC
ASI510
RSC50,51,52,53,54,56,16,17 :
Hyundai Image Quest
ASI500
E42095419
1.0
8
15


Panel Output
Damping
Network
SC_D2.5V
CSC55 104
CSC56 104
CSC57 104
CSC58 104
CSC59 104
CSC60 104
CSC61 104
CSC62 104
D2.5V
LSC51 BEAD 4532
CSC87 47uF 16V
CSC88 104
CSC89 10uF 16V
PLLVDD3
D3.3V
LSC50 BEAD 4532
CSC64 104
CSC63 104
CSC65 10uF 16V
ASI3.3V
LSC52 BEAD 4532
CSC90 104
CSC91 10uF 16V
PLLVDD1
LSC53 BEAD 4532
CSC92 104
CSC93 10uF 16V
PLLVDD2
ASI3.3V
CSC66 104
CSC67 104
CSC68 104
CSC70 104
CSC71 104
CSC72 104
CSC73 104
CSC74 104
CSC75 104
CSC76 104
CSC77 104
CSC78 104
CSC79 104
CSC80 104
CSC81 104
CSC82 104
CSC83 104
CSC84 104
CSC85 104
CSC86 104
graphic pg8 ROUT0[0..7]
RSAR01 33 ARRAY
ROUT00 ROUT01 ROUT02 ROUT03
AROUT00 AROUT01 AROUT02 AROUT03
RSAR02 33 ARRAY
ROUT04 ROUT05 ROUT06 ROUT07
AROUT04 AROUT05 AROUT06 AROUT07
AROUT0[0..7] graphic pg11
graphic pg8 GOUT0[0..7]
RSAR03 33 ARRAY
GOUT00 GOUT01 GOUT02 GOUT03
AGOUT00 AGOUT01 AGOUT02 AGOUT03
RSAR04 33 ARRAY
GOUT04 GOUT05 GOUT06 GOUT07
AGOUT04 AGOUT05 AGOUT06 AGOUT07
AGOUT0[0..7] graphic pg11
graphic pg8 BOUT0[0..7]
RSAR05 33 ARRAY
BOUT00 BOUT01 BOUT02 BOUT03
ABOUT00 ABOUT01 ABOUT02 ABOUT03
RSAR06 33 ARRAY
BOUT04 BOUT05 BOUT06 BOUT07
ABOUT04 ABOUT05 ABOUT06 ABOUT07
ABOUT0[0..7] graphic pg11
graphic pg8 ROUT1[0..7]
RSAR07 NC
ROUT10 ROUT11 ROUT12 ROUT13
RSAR08 NC
ROUT14 ROUT15 ROUT16 ROUT17
graphic pg8 GOUT1[0..7]
RSAR09 NC
GOUT10 GOUT11 GOUT12 GOUT13
RSAR10 NC
GOUT14 GOUT15 GOUT16 GOUT17
graphic pg8 BOUT1[0..7]
RSAR11 NC
BOUT10 BOUT11 BOUT12 BOUT13
RSAR12 NC
BOUT14 BOUT15 BOUT16 BOUT17
OPTION
Hyundai Image Quest
Title ASI500 Decouple Caps
Size Custom
Document Number E42095419
Rev 1.0
Date:
Sheet 9 of 15



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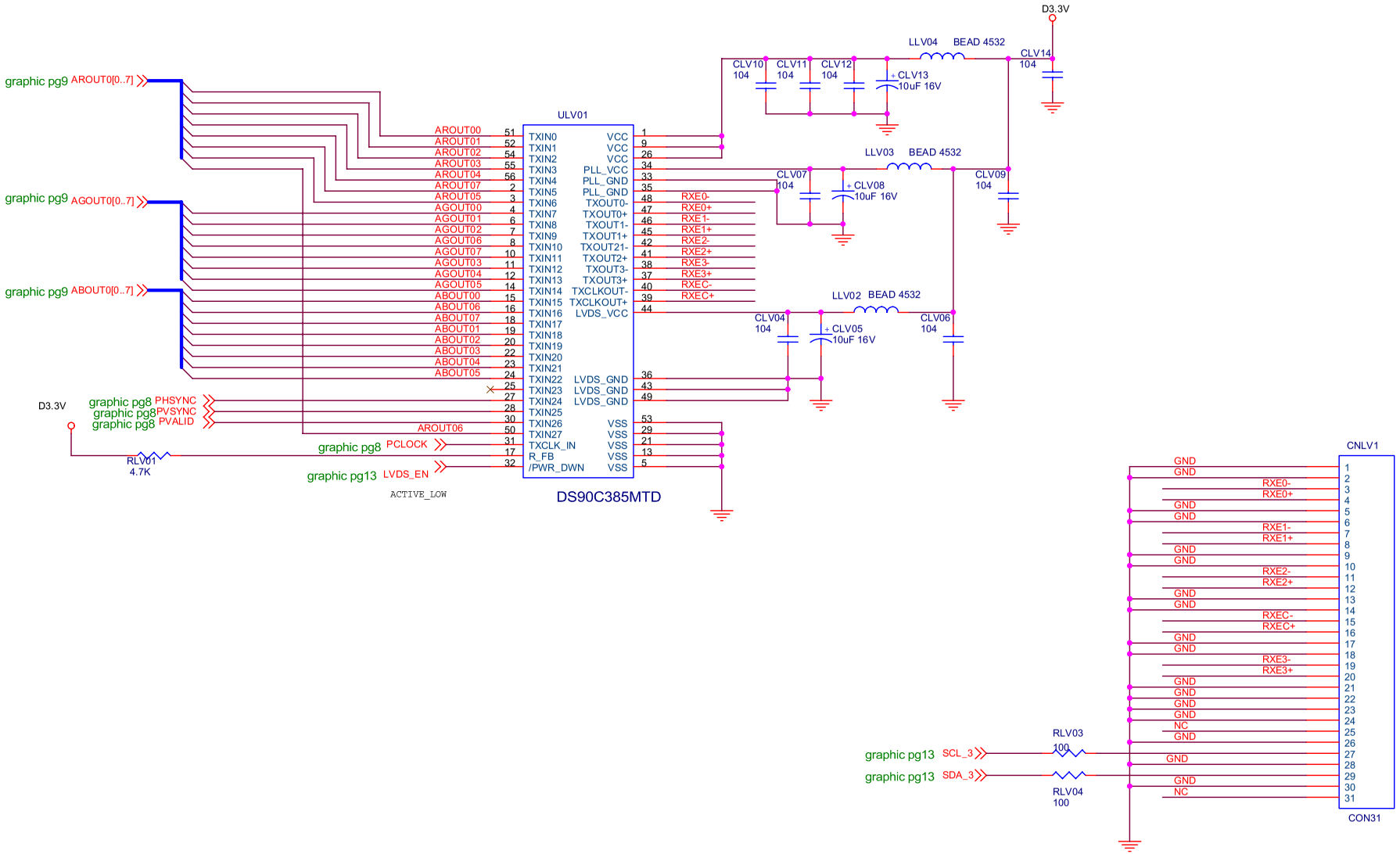
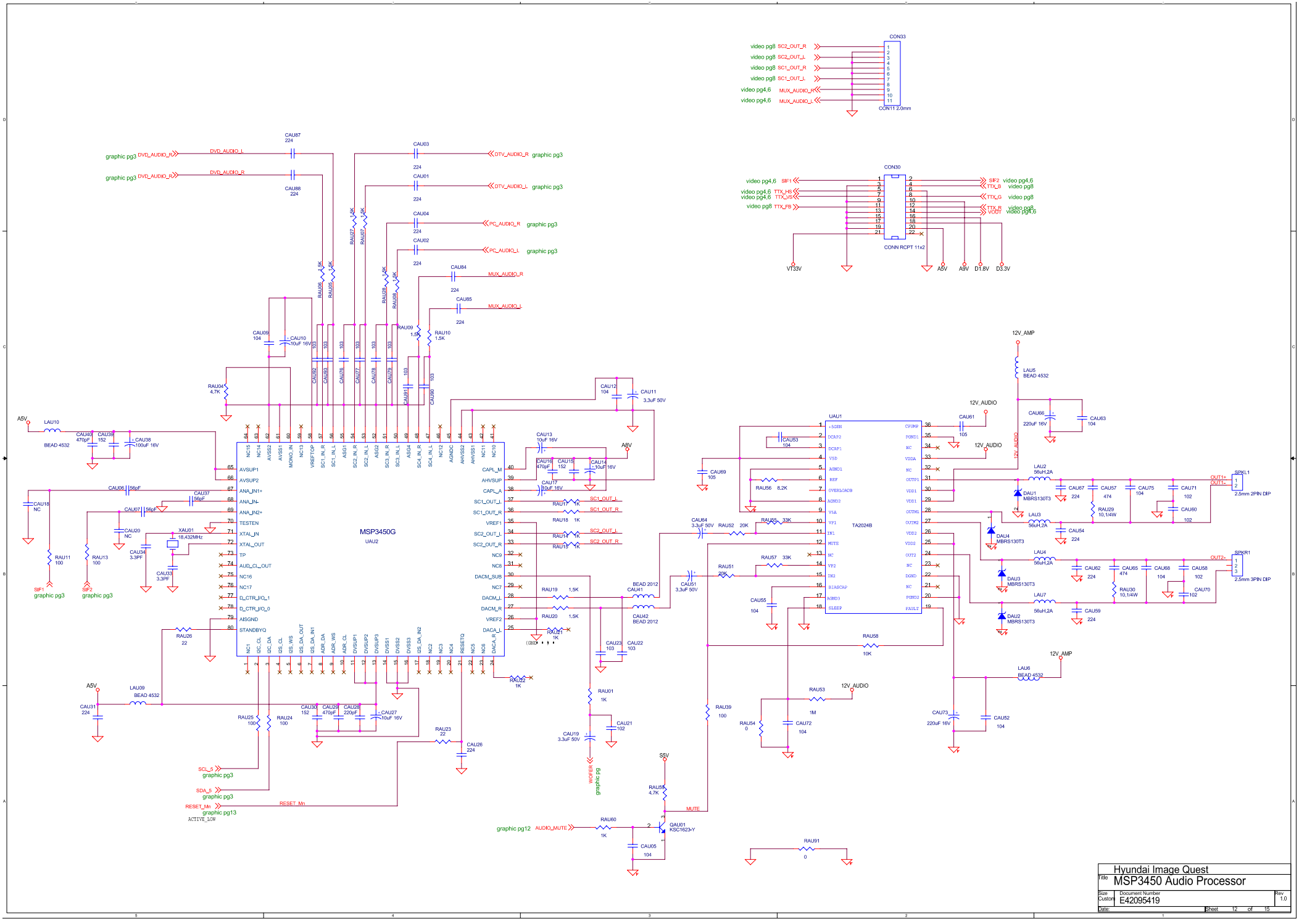
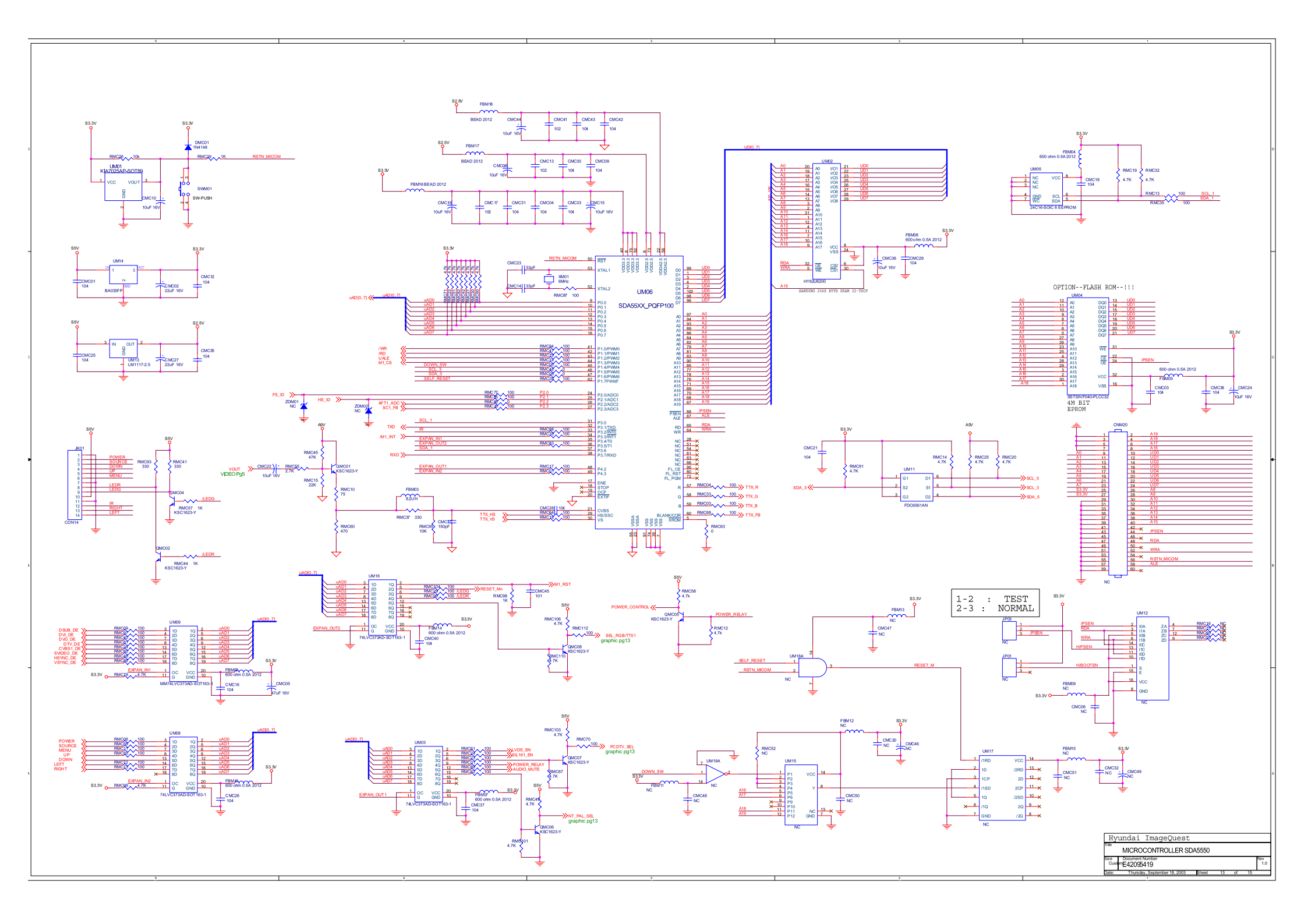
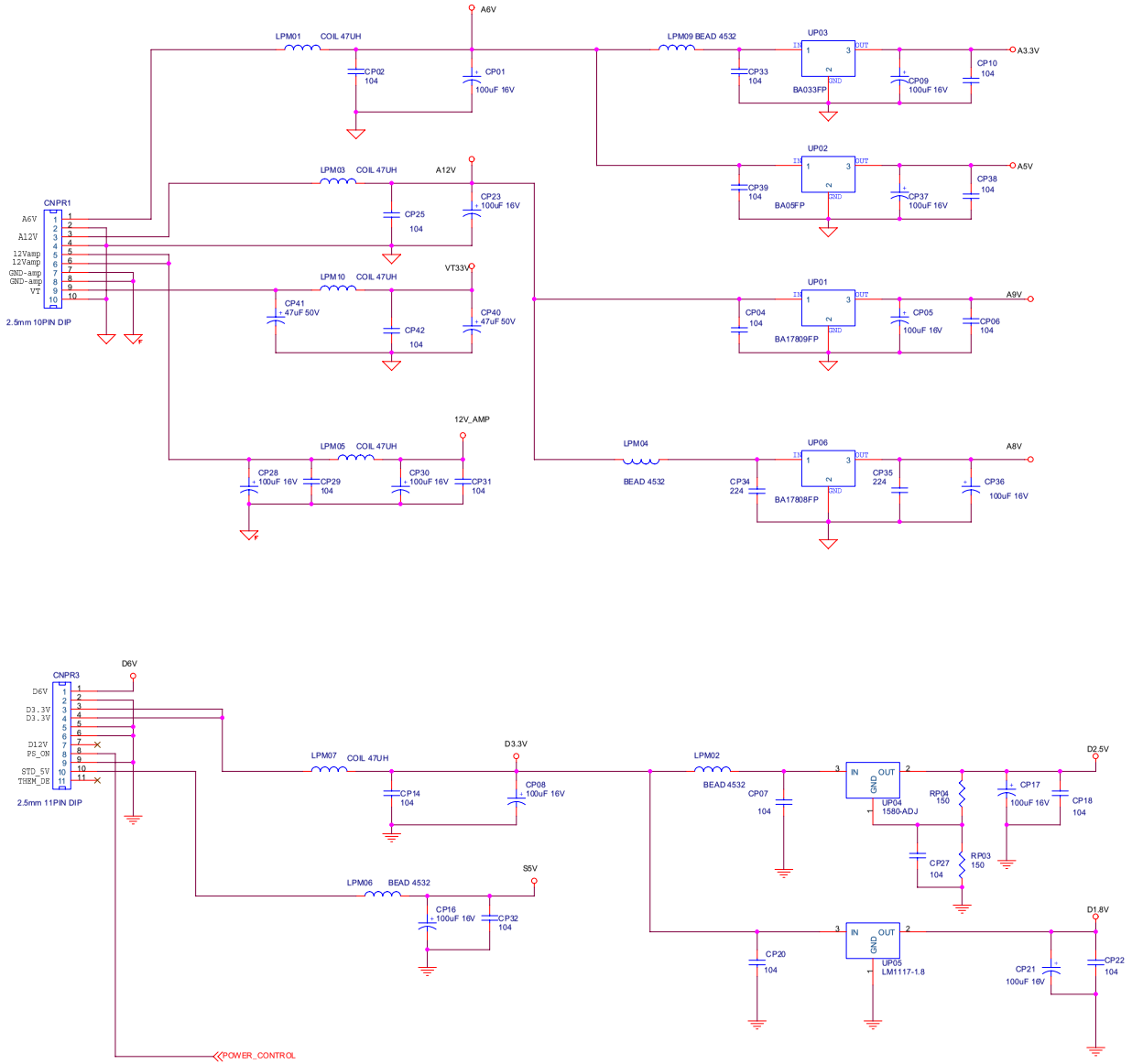
Size: Custom	Document Number: E42095419	Rev: 1.0
Date:	Sheet 10 of 15	



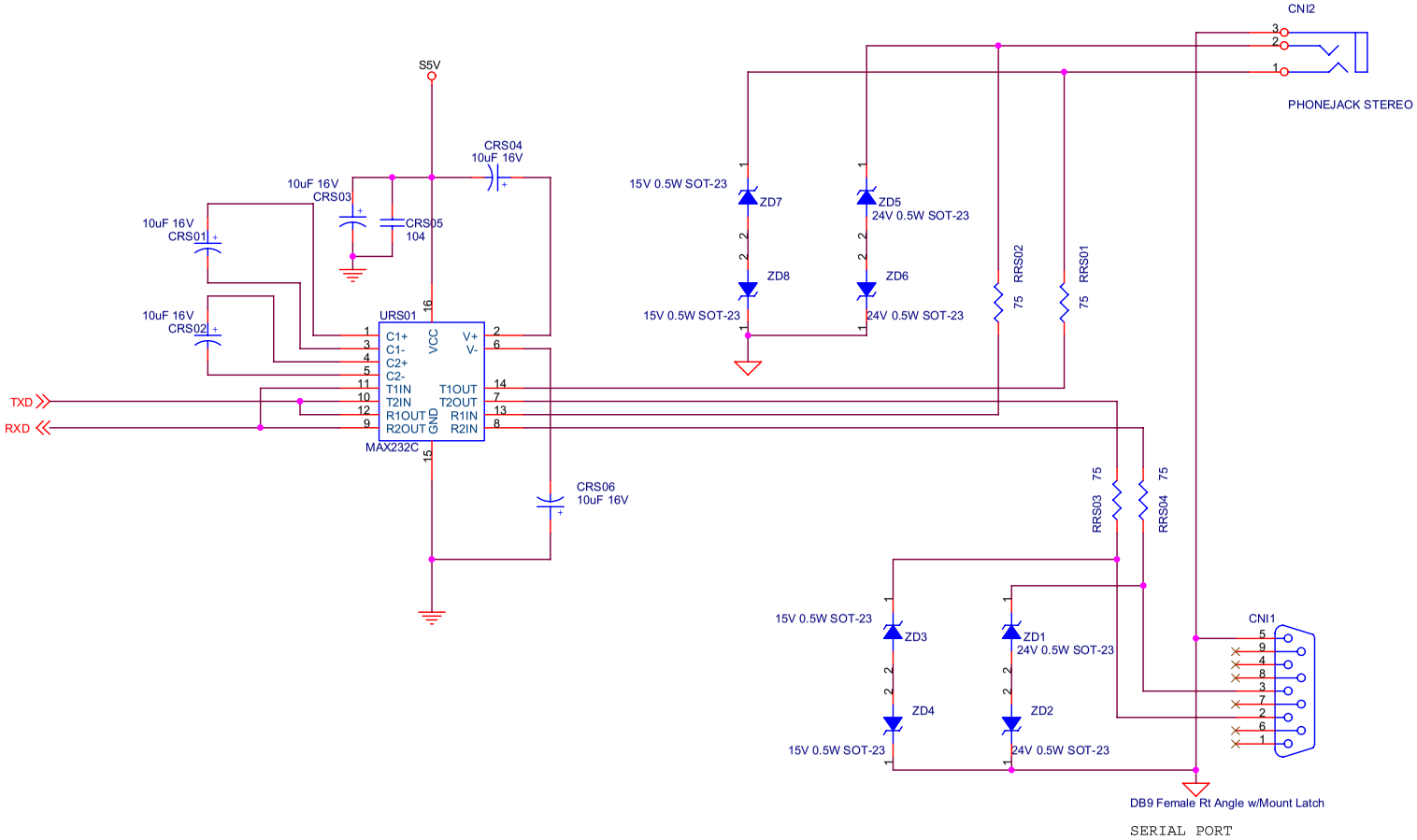
Hyundai Image Quest		
Title: LVDS Transmitter DS90C385MTD		
Size: B	Document Number: E42095419	Rev: 1.0
Date:	Sheet 11 of 15	


CON33
CON11 2.0mm
CON30
CONN RCPT 11x2
MSP3450G
UAU2
TA2024B
UAU1
Hyundai Image Quest
MSP3450 Audio Processor
E42095419
Rev 1.0
Sheet 12 of 15

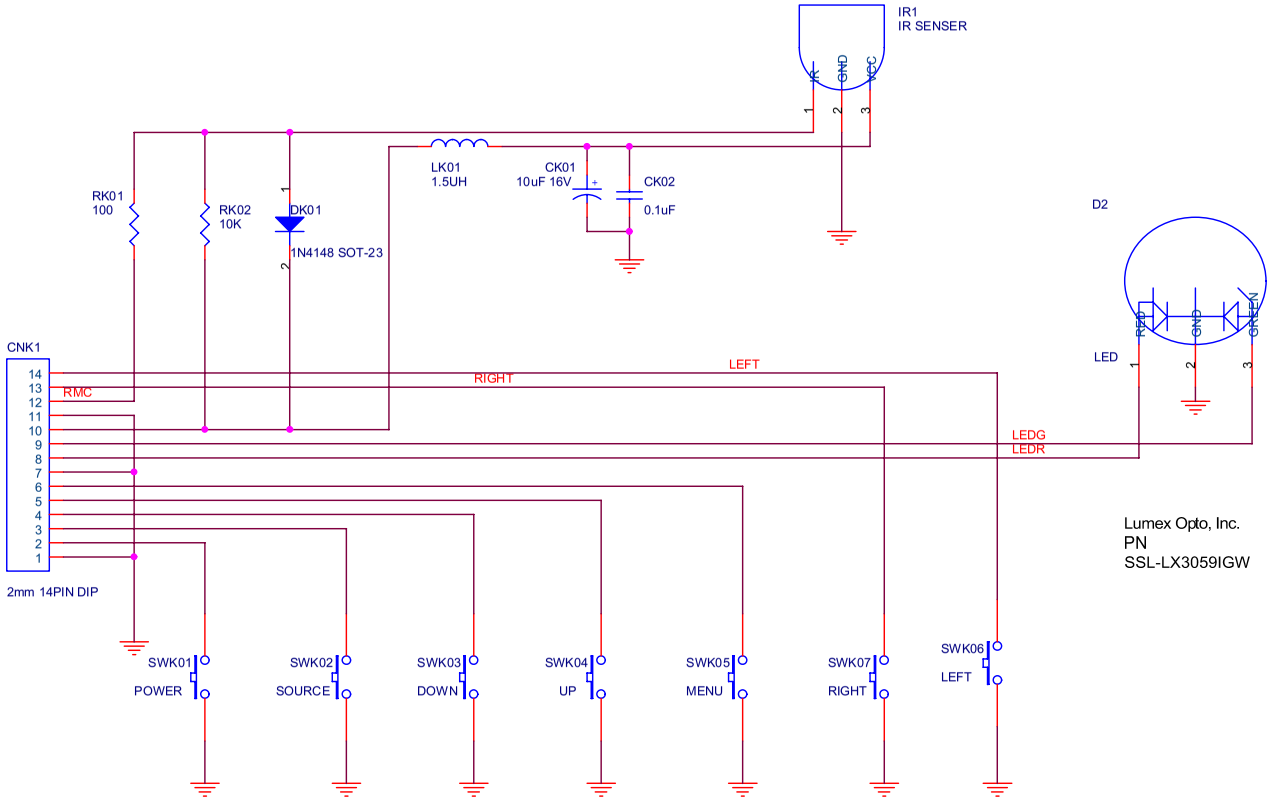

UM01
KIA7025AP-SOT89
UM14
BA033FP
UM13
LM1117-2.5
UM06
SDA55XX_PQFP100
UM02
HY62U8200
SAMSUNG 256K BYTE SRAM 32-TSOP
UM05
24C16-SOIC 8 EEPROM
UM04
SST39VF040-PLCC32
4M BIT
EPROM
OPTION--FLASH ROM--!!!
UM11
FDC6561AN
UM16
74LVC373AD-SOT163-1
UM09
MM74LVC373AD-SOT163-1
UM08
74LVC373AD-SOT163-1
UM03
74LVC373AD-SOT163-1
UM19A
UM15
UM18A
UM17
UM12
CON14
JK01
JP03
JP01
CNM20
1-2 : TEST
2-3 : NORMAL
Hyundai ImageQuest
MICROCONTROLLER SDA5550
E42095419
Thursday, September 18, 2003



Hyndai Imagequest		
Title: Power Distribution		
Size: C	Document Number: E42095419	Rev: 1.0
Date: Thursday, September 18, 2003	Sheet 14 of 15	



Hyundai ImageQuest		
Title: MAX232C		
Size: B	Document Number: E42095419	Rev: 1.0
Date: Thursday, September 18, 2003	Sheet 15 of 15	



Hyundai Image Quest		
Title: Remocon & Keypad		
Size: B	Document Number: E42095417	Rev: 1.0
Date:	Sheet 1 of 1	

Hyundai ImageQuest

PT421H

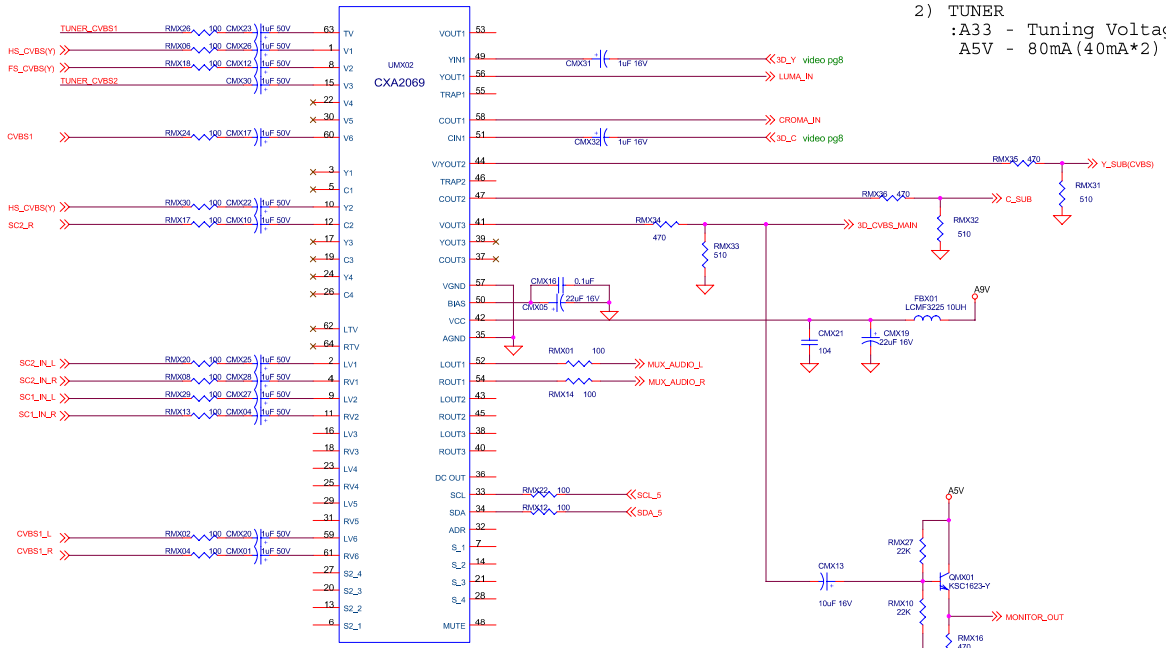
Schematic Diagram(VIDEO)

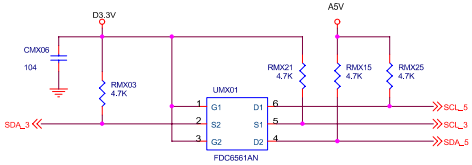
01. Cover Page
02. MUX
03. 3D COMBFILTER
04. VPC3230(MAIN)
05. VPC3230(SUB)
06. FIFO MEMORY
07. FLI2300
08. INPUT BOARD

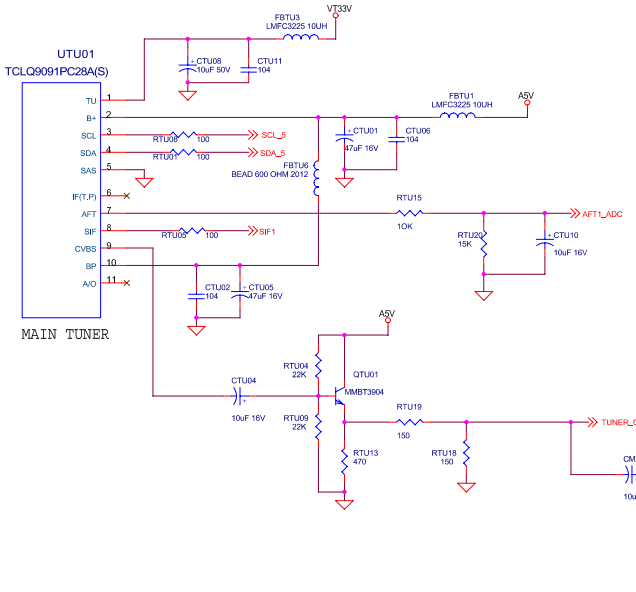
Date:05/29/2003

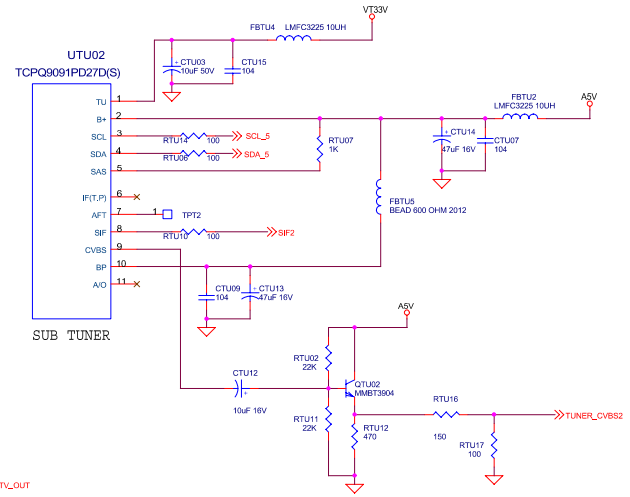
	Hyundai Image Quest
Title	PD421 SCHEMATIC DIAGRAM
Size: B	Document Number: E42095417
Rev: 1.0	
Date:	Sheet 1 of 08

1) CXA2069
   :A5V - 72mA
2) TUNER
   :A33 - Tuning Voltage
    A5V - 80mA(40mA*2)

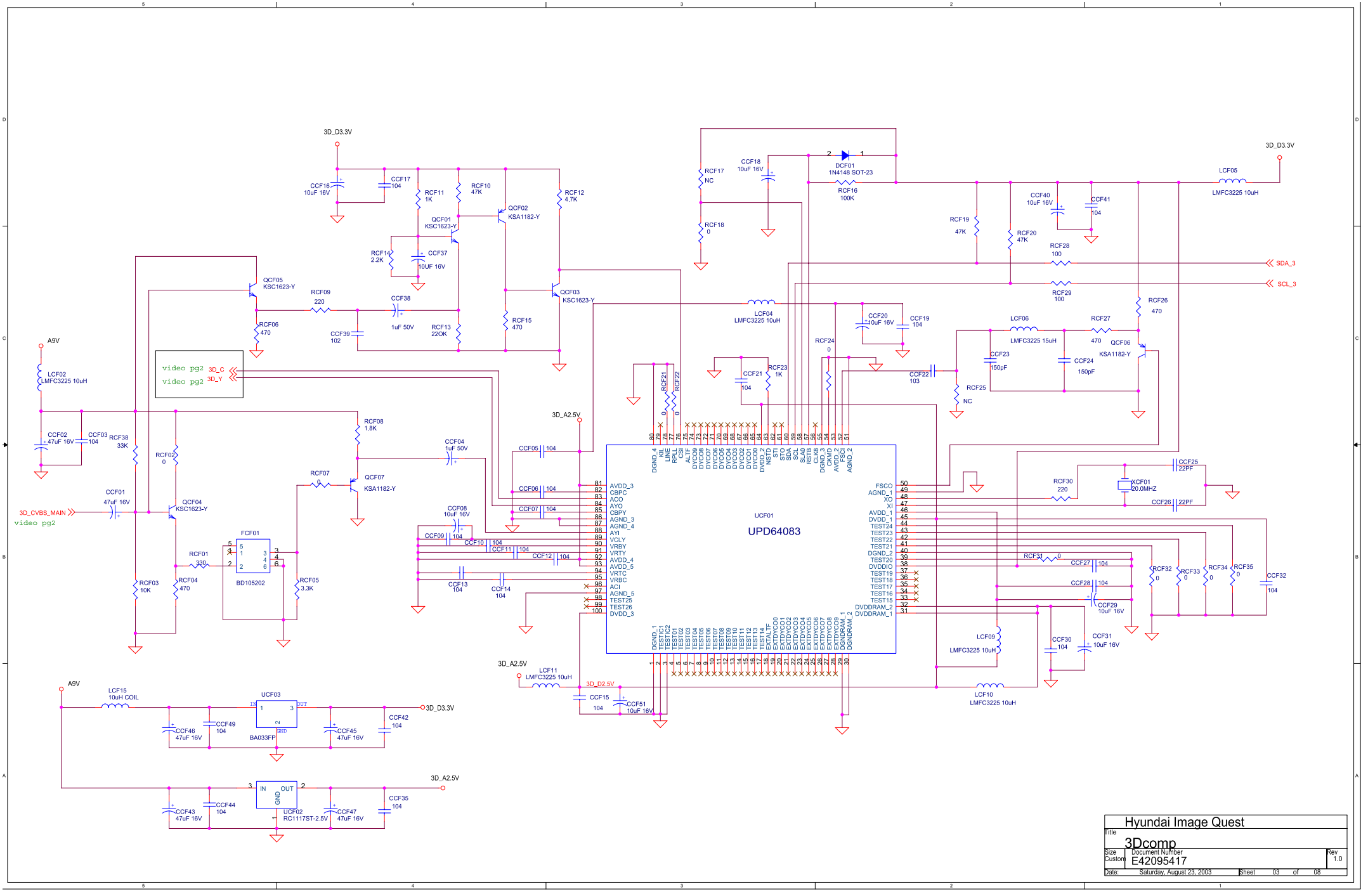


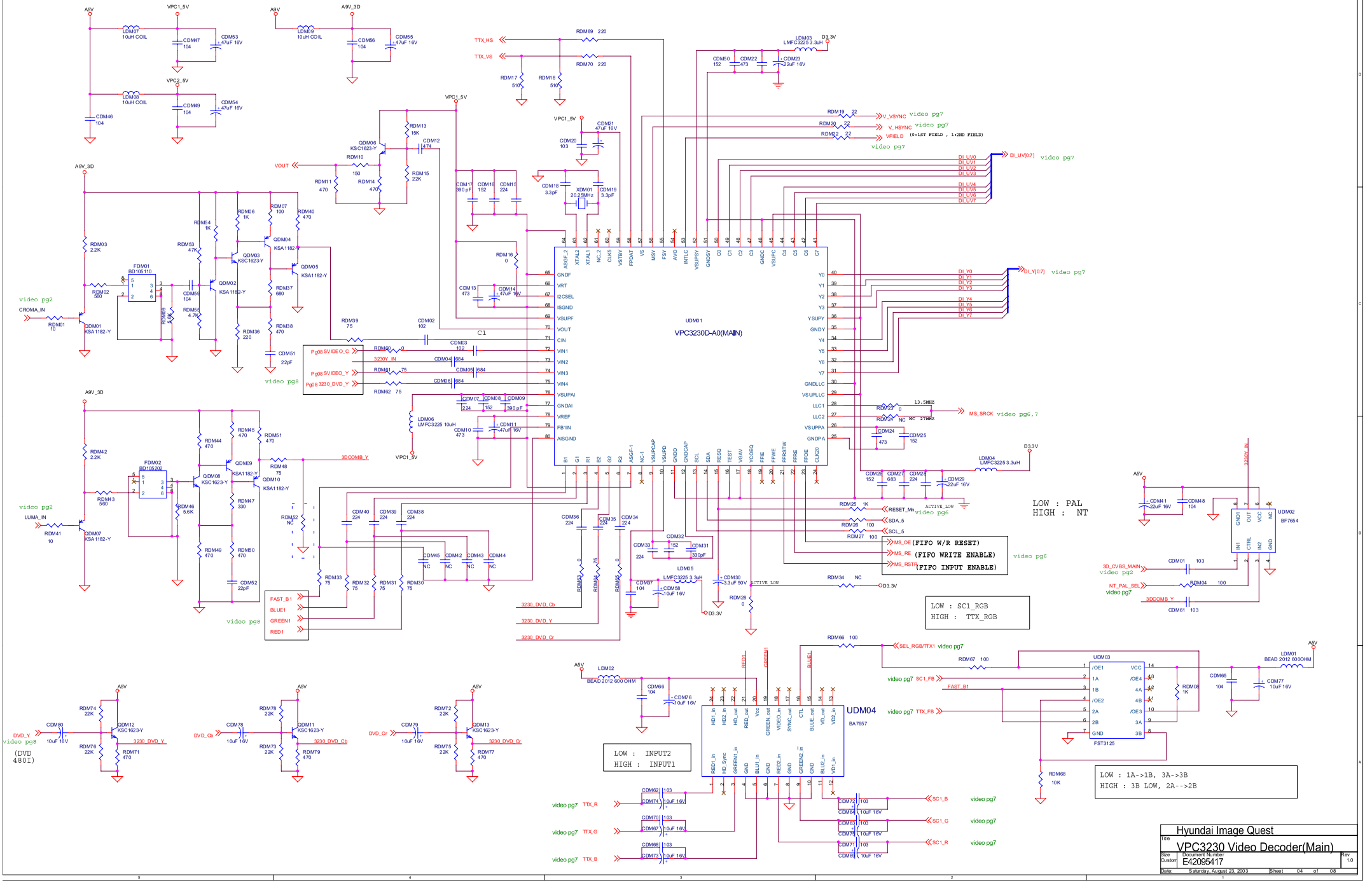


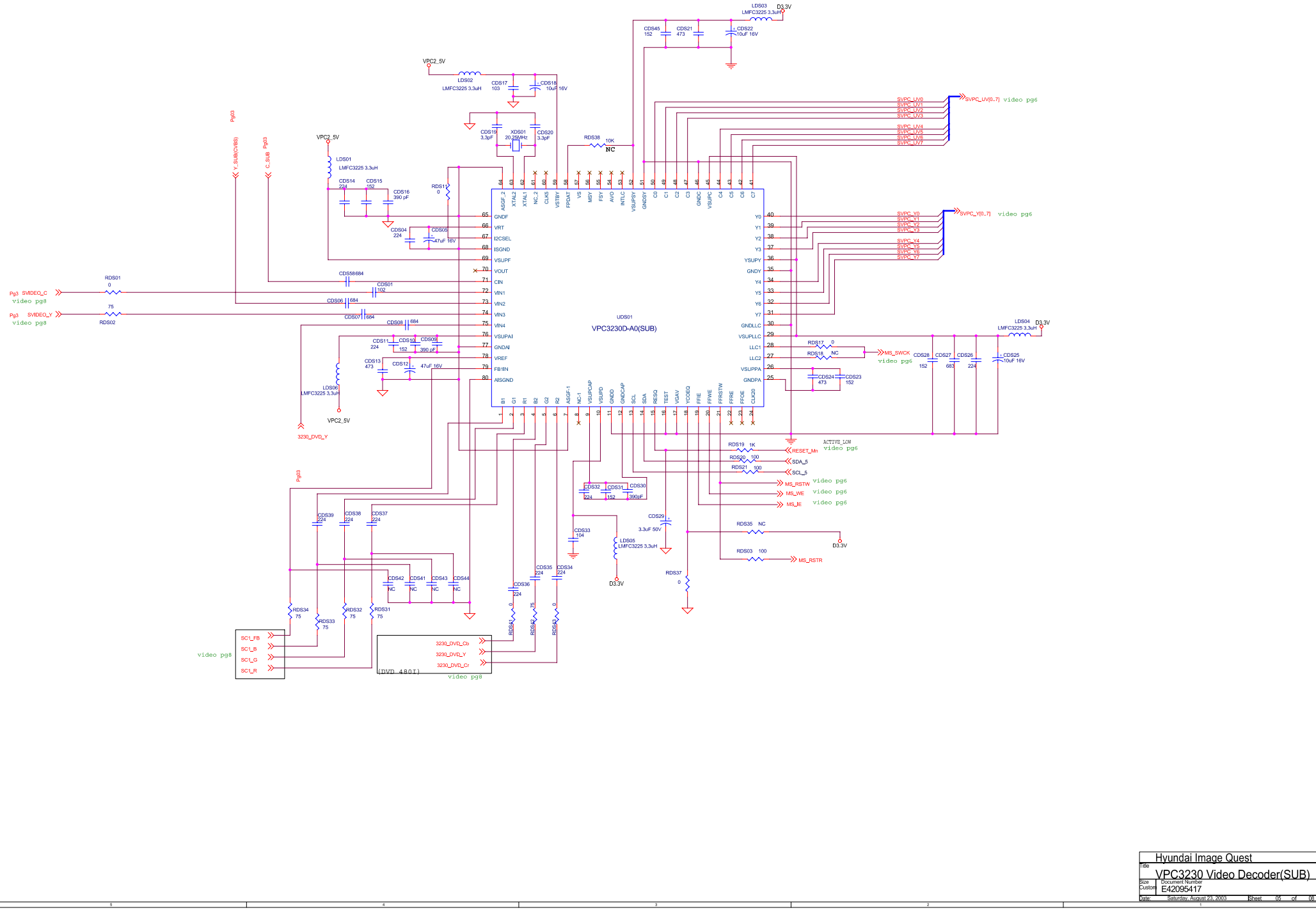


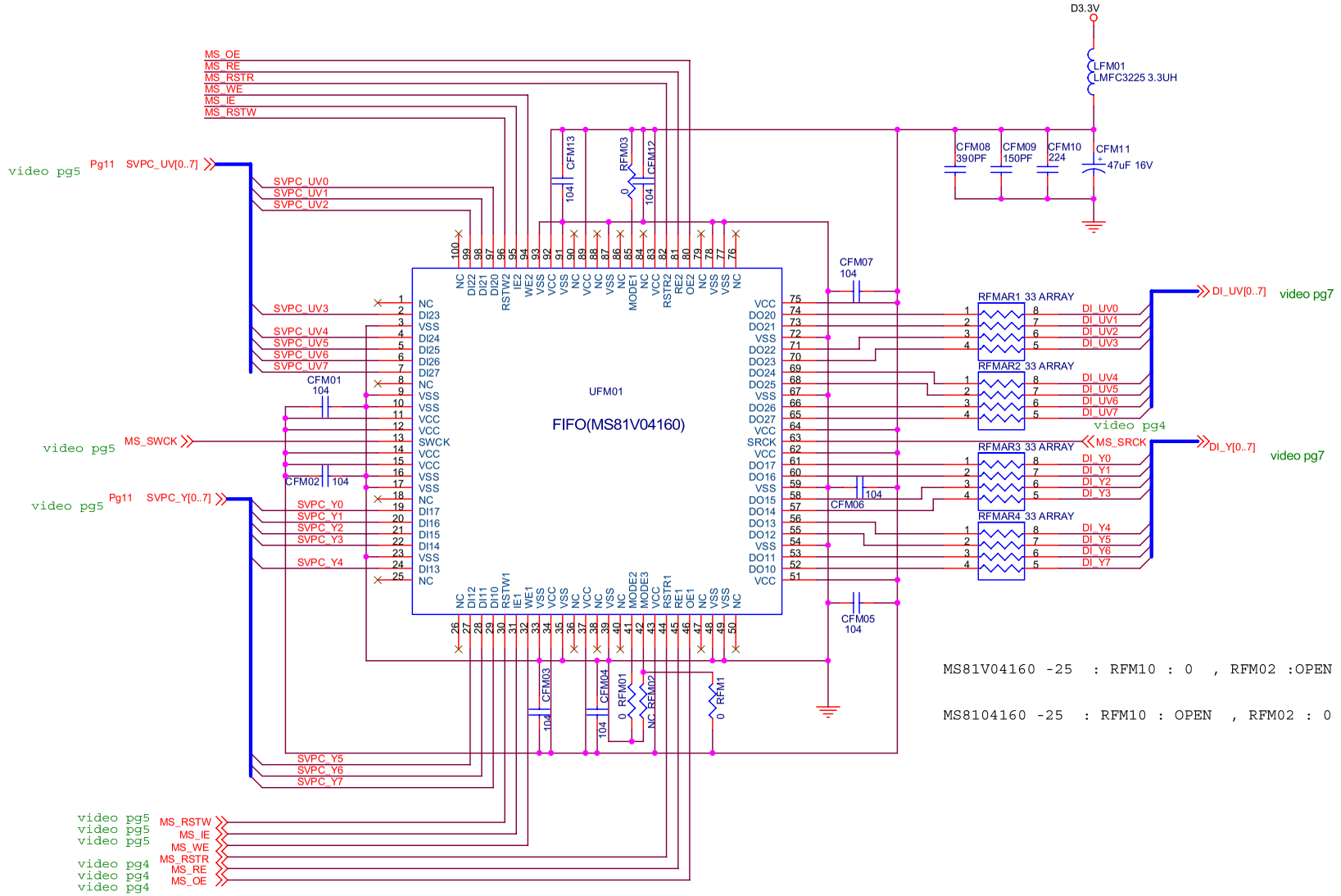


Title	TUNER & CXA2069 & CONN		
Size	Document Number		Rev
Custom	<Doc>		<RevCode>
Date:	Thursday, August 28, 2003	Sheet 2 of 08	

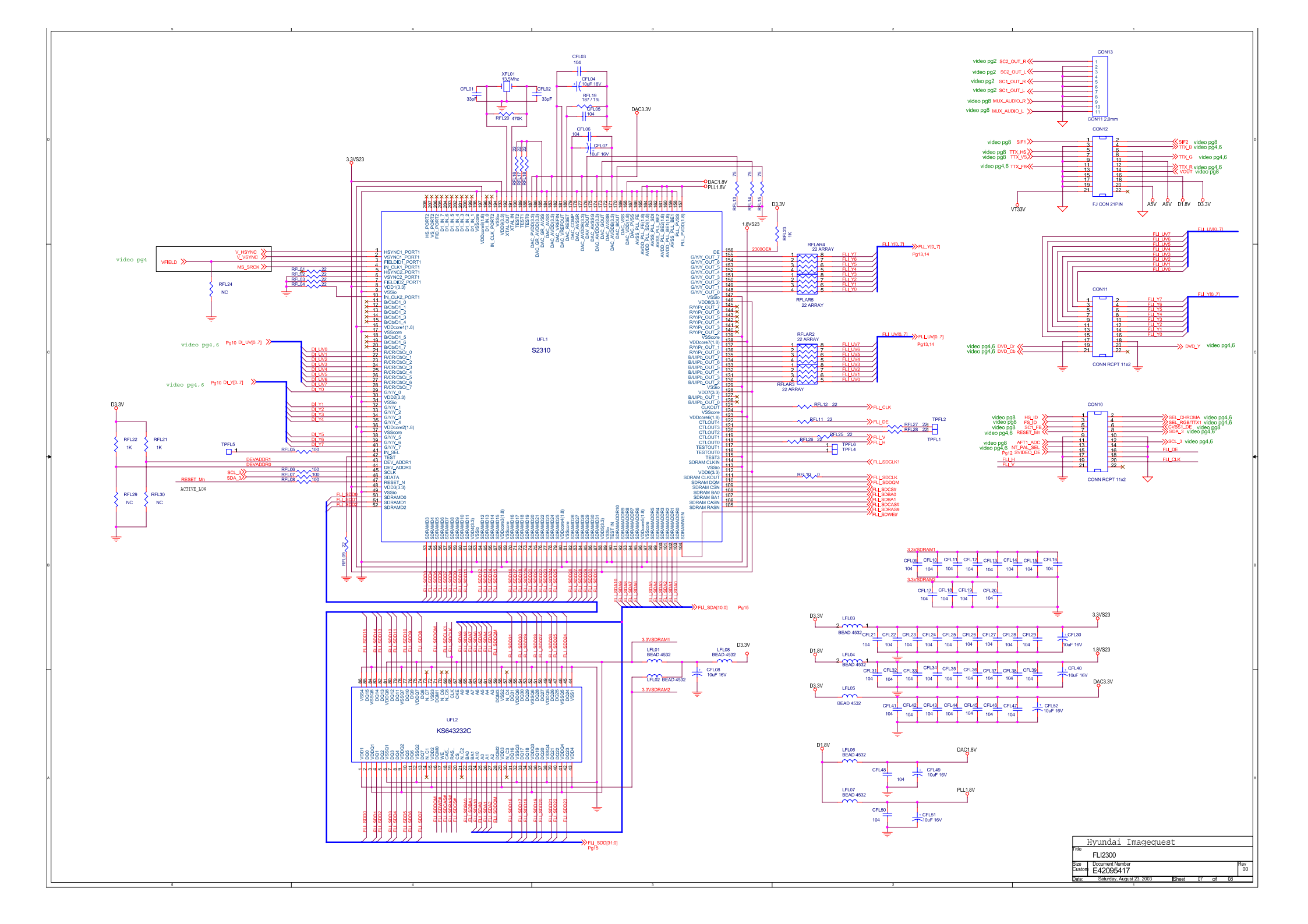

UCF01
UPD64083
3D_D3.3V
3D_A2.5V
3D_D2.5V
A9V
video pg2
3D_C
3D_Y
3D_CVBS_MAIN
SDA_3
SCL_3
BD105202
BA033FP
RC1117ST-2.5V
Hyundai Image Quest
3Dcomp
E42095417
Saturday, August 23, 2003
Sheet 03 of 08


UDM01
VPC3230D-A0(MAIN)
UDM04
BA7657
UDM03
FST3125
UDM02
BF7654
LOW : PAL
HIGH : NT
(FIFO W/R RESET)
(FIFO WRITE ENABLE)
(FIFO INPUT ENABLE)
LOW : SC1_RGB
HIGH : TTX_RGB
LOW : INPUT2
HIGH : INPUT1
LOW : 1A->1B, 3A->3B
HIGH : 3B LOW, 2A-->2B
Hyundai Image Quest
VPC3230 Video Decoder(Main)
E42095417
Saturday, August 23, 2003


UDS01
VPC3230D-A0(SUB)
LDS03 D3.3V LMFC3225 3.3uH
LDS02 LMFC3225 3.3uH
LDS01 LMFC3225 3.3uH
LDS04 D3.3V LMFC3225 3.3uH
LDS05 LMFC3225 3.3uH
LDS06 LMFC3225 3.3uH
VPC2_5V
D3.3V
XDS01 20.250MHz
RDS38 10K NC
SVPC_UV[0..7] video pg6
SVPC_Y[0..7] video pg6
MS_SWCK video pg6
RESET_M video pg6
ACTIVE_LOW
SDA_5
SCL_5
MS_RSTW video pg6
MS_WE video pg6
MS_JE video pg6
MS_RSTR
Y_SUB(CVBS) Pg3
C_SUB Pg3
Pg3 SVIDEO_C video pg8
Pg3 SVIDEO_Y video pg8
3230_DVD_Y
3230_DVD_Cb
3230_DVD_Cr
(DVD 480I)
video pg8
SC1_FB
SC1_B
SC1_G
SC1_R
Hyundai Image Quest
VPC3230 Video Decoder(SUB)
E42096417
Saturday, August 23, 2003
Sheet 05 of 08



Hyundai Image Quest		
Title: FIFO Memory		
Size: B	Document Number: E42095417	Rev: 1.0
Date:	Sheet 06 of 08	


UFL1
S2310
UFL2
KS643232C
XFL01
15.0Mhz
CFL01
33pF
CFL02
33pF
RFL20 470K
CFL03
104
CFL04
10uF 16V
RFL19
187 / 1%
CFL05
104
CFL06
104
CFL07
10uF 16V
DAC3.3V
DAC1.8V
PLL1.8V
3.3VS23
1.8VS23
D3.3V
RFL23
1K
RFLAR4
22 ARRAY
RFLAR5
22 ARRAY
RFLAR2
22 ARRAY
RFLAR3
22 ARRAY
2300QE#
FLI_Y[0..7]
Pg13,14
FLI_UV[0..7]
Pg13,14
video pg4
V_HSYNC
V_VSYNC
FIELDID
MS_SRCK
RFL24
NC
video pg4,6
Pg10 DI_UV[0..7]
Pg10 DI_Y[0..7]
DI_UV0
DI_UV1
DI_UV2
DI_UV3
DI_UV4
DI_UV5
DI_UV6
DI_UV7
DI_Y0
DI_Y1
DI_Y2
DI_Y3
DI_Y4
DI_Y5
DI_Y6
DI_Y7
RFL05
100
TPFL5
DEVADDR1
DEVADDR0
RFL06
RFL07
RFL08
SCL_3
SDA_3
RESET_Mn
ACTIVE_LOW
RFL22
1K
RFL21
1K
RFL29
NC
RFL30
NC
RFL09
22
FLI_SDD0
FLI_SDD1
FLI_SDD2
RFL12 22
RFL11 22
RFL26 22
RFL25 22
RFL27 22
RFL28 22
TPFL2
TPFL1
TPFL6
TPFL4
RFL10 0
FLI_CLK
FLI_DE
FLI_V
FLI_H
FLI_SDCLK1
FLI_SDCLK
FLI_SDDQM
FLI_SDCS#
FLI_SDBA0
FLI_SDBA1
FLI_SDCAS#
FLI_SDRAS#
FLI_SDWE#
FLI_SDA[10:0]
Pg15
FLI_SDD[31:0]
Pg15
3.3VSDRAM1
3.3VSDRAM2
LFL01
BEAD 4532
LFL02 BEAD 4532
LFL08
BEAD 4532
CFL08
10uF 16V
CON13
CON11 2.0mm
video pg2 SC2_OUT_R
video pg2 SC2_OUT_L
video pg2 SC1_OUT_R
video pg2 SC1_OUT_L
video pg8 MUX_AUDIO_R
video pg8 MUX_AUDIO_L
CON12
FJ CON 21PIN
video pg8 SIF1
video pg8 TTX_HS
video pg8 TTX_VS
video pg4,6 TTX_FB
SIF2 video pg8
TTX_B video pg4,6
TTX_G video pg4,6
TTX_R video pg4,6
VOUT video pg8
VT33V
A5V
A9V
D1.8V
D3.3V
CON11
CONN RCPT 11x2
video pg4,6 DVD_Cr
video pg4,6 DVD_Cb
DVD_Y video pg4,6
CON10
CONN RCPT 11x2
video pg8 HS_ID
video pg8 FS_ID
video pg8 SC1_FB
video pg4,6 RESET_Mn
video pg8 AFT1_ADC
video pg4,6 NT_PAL_SEL
Pg12 SVIDEO_DE
SEL_CHROMA video pg4,6
SEL_RGBTTX1 video pg4,6
CVBS1_DE video pg8
SDA_3 video pg4,6
SCL_3 video pg4,6
FLI_DE
FLI_CLK
FLI_H
FLI_V
LFL03
BEAD 4532
LFL04
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LFL05
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LFL07
BEAD 4532
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10uF 16V
CFL40
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CFL52
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DAC1.8V
PLL1.8V
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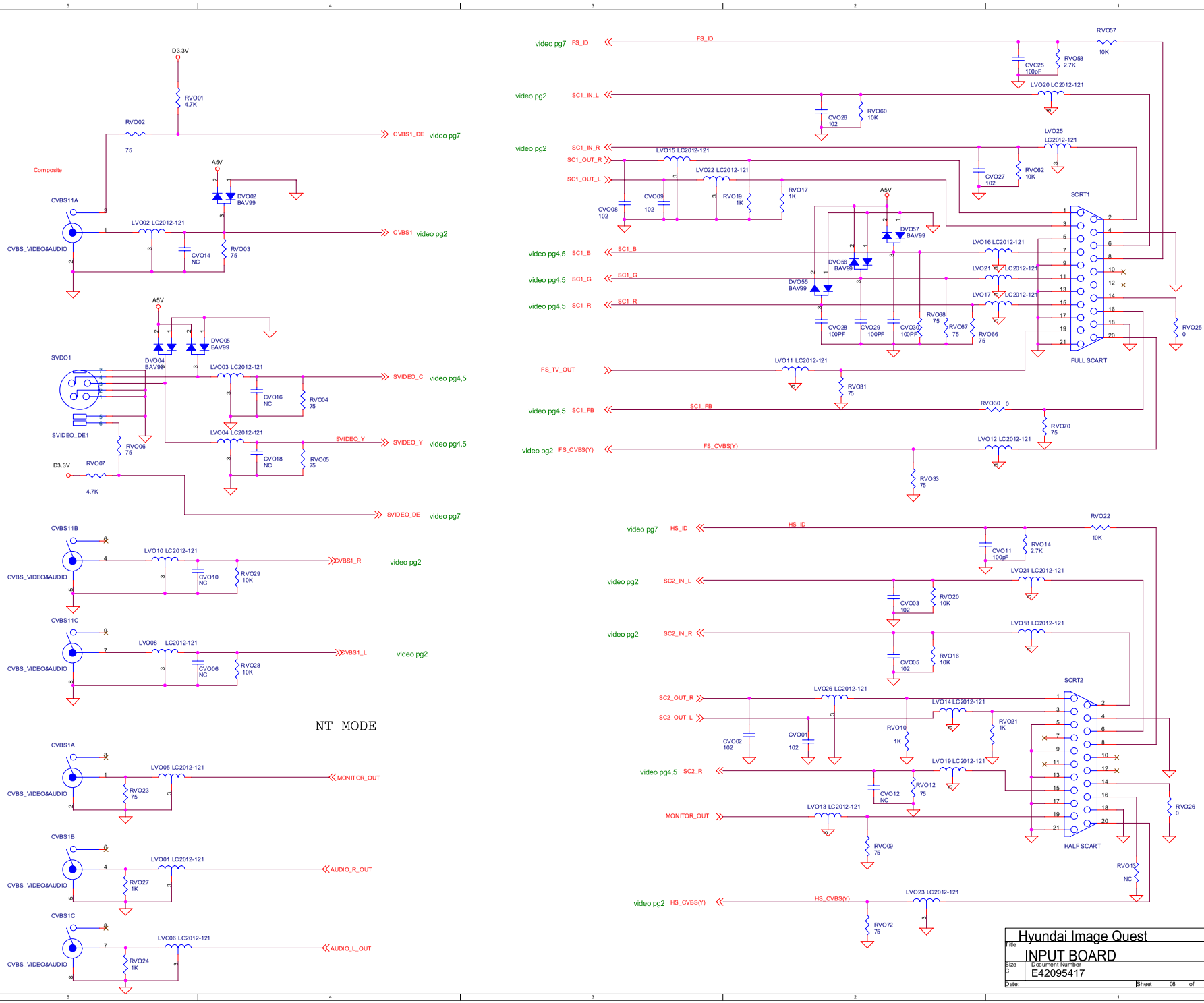
Sheet
07
of
08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Composite
A5V
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CVBS11A
CVBS_VIDEO&AUDIO
LVO02 LC2012-121
CVO14 NC
RVO03 75
CVBS1 video pg2
SVDO1
DVO04 BAV99
DVO05 BAV99
LVO03 LC2012-121
CVO16 NC
RVO04 75
SVIDEO_C video pg4,5
SVIDEO_DE1
RVO06 75
LVO04 LC2012-121
CVO18 NC
RVO05 75
SVIDEO_Y video pg4,5
D3.3V
RVO07 4.7K
SVIDEO_DE video pg7
CVBS11B
LVO10 LC2012-121
CVO10 NC
RVO29 10K
CVBS1_R video pg2
CVBS11C
LVO08 LC2012-121
CVO06 NC
RVO28 10K
CVBS1_L video pg2
NT MODE
CVBS1A
LVO05 LC2012-121
RVO23 75
MONITOR_OUT
CVBS1B
LVO01 LC2012-121
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AUDIO_R_OUT
CVBS1C
LVO06 LC2012-121
RVO24 1K
AUDIO_L_OUT
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RVO57 10K
CVO25 100pF
RVO58 2.7K
LVO20 LC2012-121
video pg2 SC1_IN_L
CVO26 102
RVO60 10K
video pg2 SC1_IN_R
SC1_OUT_R
SC1_OUT_L
LVO15 LC2012-121
LVO22 LC2012-121
LVO25 LC2012-121
CVO27 102
RVO62 10K
CVO08 102
CVO09 102
RVO19 1K
RVO17 1K
A5V
DVO57 BAV99
SCRT1
video pg4,5 SC1_B
SC1_B
LVO16 LC2012-121
video pg4,5 SC1_G
SC1_G
DVO56 BAV99
LVO21 LC2012-121
video pg4,5 SC1_R
SC1_R
DVO55 BAV99
LVO17 LC2012-121
CVO28 100PF
CVO29 100PF
CVO30 100PF
RVO68 75
RVO67 75
RVO66 75
FULL SCART
RVO25 0
FS_TV_OUT
LVO11 LC2012-121
RVO31 75
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SC1_FB
RVO30 0
RVO70 75
video pg2 FS_CVBS(Y)
FS_CVBS(Y)
LVO12 LC2012-121
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video pg7 HS_ID
HS_ID
RVO22 10K
CVO11 100pF
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video pg2 SC2_IN_L
CVO03 102
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video pg2 SC2_IN_R
LVO18 LC2012-121
CVO05 102
RVO16 10K
SCRT2
SC2_OUT_R
SC2_OUT_L
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LVO14 LC2012-121
CVO02 102
CVO01 102
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RVO21 1K
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CVO12 NC
RVO12 75
MONITOR_OUT
LVO13 LC2012-121
RVO09 75
HALF SCART
RVO26 0
RVO13 NC
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HS_CVBS(Y)
LVO23 LC2012-121
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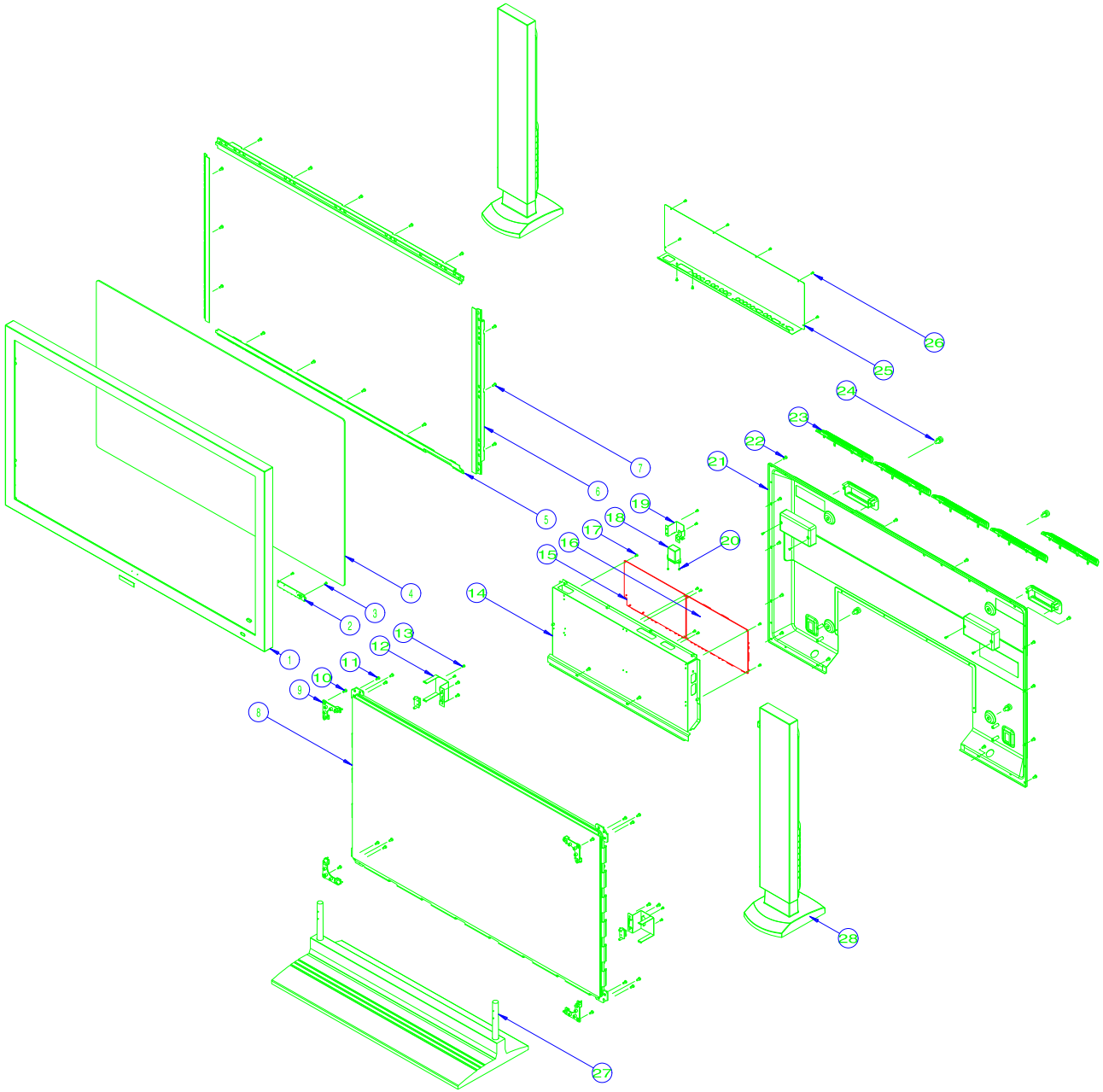
Hyundai Image Quest
Title
INPUT BOARD
Size C
Document Number
E42095417
Rev 1.0
Date:
Sheet 08 of 08



NO.	PART NO.	PART NAME	DESCRIPION	QT'Y	REMARK
28		SPEAKER ASSY PD421	PC+ABS 94-V0	2	
27		STAND ASSY PD421		1	
26	5001000579	SCR-MC BIN MC3X8		9	
25	3010100140	SHIELD TOP PD421	A5052P T=1.0	1	
24	5004000219	SCR-MC BIN+MC 8X14		4	
23	6201326600	REAR COVER CAP PD421	ABS 94-HB	5	
22	5004000217	SCR-TT BIN MC4*10			
21	6101221200	REAR COVER ASSY PD421	A5052P T=1.0	1	
20	M11173008012	SCREW FLT(+) M3x8 MSZPC		2	
19	6110282200	BRKT AC INLET	SECC T=1.0	1	
18	3725005299	NOISE FILTER CABLE		1	
17	5004000218	SCR-MC BIN+MC 3X16		7	
16		GRAPHIC BOARD ASSY		1	
15		A/V BOARD ASSY		1	
14	6120055400	SHIELD BOTTOM ASSY	A5052P T=1.0	1	
13	5004000190	SCR-TT BIN+MC 3X8		8	
12	6110280100	SPEAKER BRKT JACK PD421	SECC T=1.0	2	
11	M11144010012	SCR BIN(+) 4X10 MSZPC		12	
10	5004000187	SCR TT2 BIN+MC 4X14			
9	6120055000	MODULE PLATE	ALDC 12S	4	
8	3011200001	PDP S42SD-YDXX PD421		1	
7	5004000217	SCR-TT BIN MC4*10		23	
6	61102824/2500	FILTER BRKT V ASSY	A1050P T=1.5	2	
5	61102822/2300	FILTER BRKT H ASSY	A1050P T=1.5	2	
4	6120055300	FILTER GLASS PD421		1	
3	5004000190	SCR-TT BIN+MC 3X8		8	
2	301070082701	KEY BOARD ASSY PD421		1	
1	6201319400	COVER FRONT ASSY	PC+ABS	1	

DRAWN BY: S.K.KWAG 2003.06.25	PLANNED BY:	CHECKED BY:	APPROVED BY:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN mm (INCHES) TOLERANCES ARE: LINEAR ± ANGLES ± RADII UNLESS NOTED±	ANGLE 3rd
IMAGEQUEST				MDL. PD421 REF NO.	SIZE A2

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SCALE 1/1
DWG NO. B4210013701A
REV A
SHEET 1/1
FILE NAME : EXPLODED VIEW